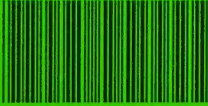


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FR-10 AND FR-20
TELEVISION SYNC
SIGNAL GENERATORS

INSTRUCTION MANUAL

FAIRCHILD

SPACE AND DEFENSE SYSTEMS

A DIVISION OF FAIRCHILD CAMERA AND INSTRUMENT CORPORATION

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The Space and Defense Systems Division warrants that each new TV Camera and other Electronic or Electrical Supplementary TV Camera Equipment (hereinafter referred to as "Instrument") manufactured or sold by it, is free from defects in material or workmanship under normal use and service for a period of one year from the date of its sale to the first purchaser for use. If, upon examination by Fairchild, the Instrument is determined to be defective in workmanship or material, Fairchild will, subject to the conditions set forth below, either repair the defective part or replace it with a new part. Fairchild shall not be liable for any delay or failure to furnish a replacement part resulting directly or indirectly from any governmental restriction, priority or allocation or any other governmental regulatory order or action, nor shall Fairchild be liable for damages by reason of the failure of the Instrument to perform properly or for any consequential damages. This warranty does not apply to any Instrument that has been subject to negligence, accident, misuse or improper installation or operation or that in any way has been tampered with, altered or repaired by any person other than an authorized Fairchild service organization or any employee thereof, or to any Instrument whose serial number has been altered, defaced or removed, or to any Instrument purchased within, and thereafter removed beyond the continental limits of the United States.

This warranty shall, at Fairchild's option, become void unless registration thereof is promptly effected as provided below. This warranty is in lieu of all other warranties, expressed or implied, and no one is authorized to assume any liability on behalf of Fairchild or impose any obligation upon it in connection with the sale of any Instrument, other than as stated above.

REGISTERING THE WARRANTY

To register this warranty, the warranty registration card enclosed with the Instrument must be properly filled out and mailed to the Space and Defense Systems Division immediately upon receipt of the equipment. Complete information is necessary. BOTH THE TYPE NUMBER AND THE SERIAL NUMBER OF THE INSTRUMENT MUST BE GIVEN ON THIS CARD. Instruments must be examined immediately upon receipt, since claims for damage in transit will not be honored by the carrier unless prompt action is taken.

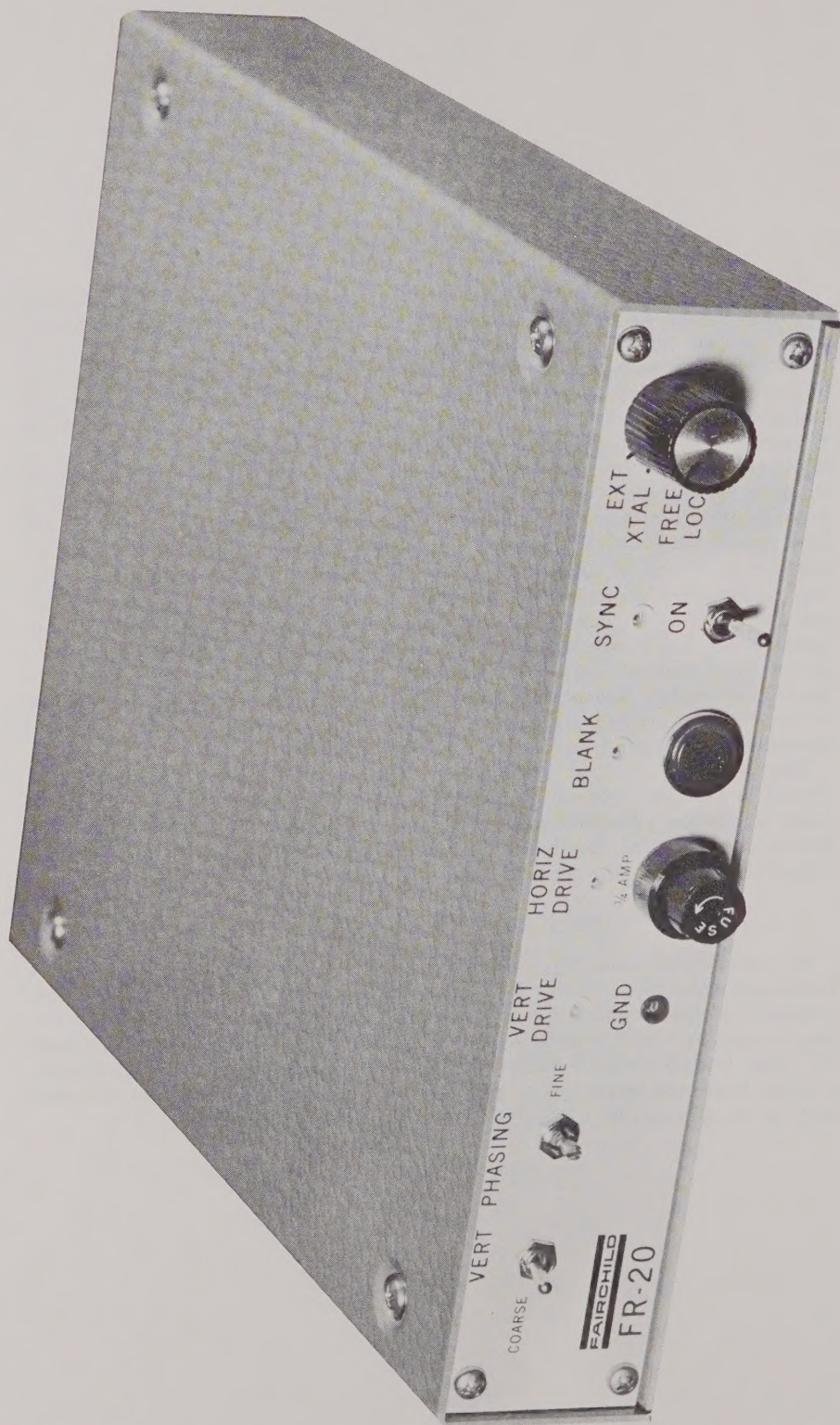


Figure 1-1. FR-20 Television Synchronizing Signal Generator

SECTION I

DESCRIPTION

1-1. GENERAL

The Fairchild Television Synchronizing Signal Generator Models FR-10 and FR-20 provide standard EIA synchronizing, blanking, and drive signals for use with commercial, military, and industrial television systems. The generator is available in many different line/frame rate modes of operation. The particular line/frame rate is as specified by the customer at the time of purchase.

1-2. MODEL DIFFERENCES

The Model FR-10 consists of a printed circuit board containing a master oscillator, counting, and pulse generating circuits; it also includes the necessary power supply rectifying, filtering, and voltage regulating circuits, but does not include a power transformer. The Model FR-10 is installed in other Fairchild equipment from which it obtains its power supply ac voltages.

The Model FR-20 (figure 1-1) is a self-contained television synchronizing signal generator suitable for mounting in a rack or on a shelf. It consists of the Model FR-10 enclosed in a small two-piece cabinet, which also includes a power supply transformer, a vertical phasing circuit, rear panel coaxial connectors, and front panel controls and test points. The cabinet consists of an epoxy finished wrap-around top cover and a flat base plate. The top cover is secured by four screws, and the base plate is secured by the same four screws that attach the rubber mounting feet. Optional kits are available to permit mounting single or dual (side-by-side) FR-20 units in a standard 19-inch rack.

Except for ac power and the vertical phasing circuit, both models are electrically the same.

Models equipped with optional crystal control are designated by a "C" suffix (e.g., FR-20/C).

The line/frame rate of each model is marked on a blue line rate jumper plug (P11) located on top of the printed circuit board.

1-3. TECHNICAL SUMMARY

Table 1-1 lists the electrical, environmental, and mechanical characteristics for Models FR-10 and FR-20 Television Sync Signal Generators.

1-4. OPTIONAL EQUIPMENT

Table 1-2 lists optional equipment available for use with the FR-10 and FR-20 Television Sync Signal Generators.

TABLE 1-1
TECHNICAL SUMMARY

Electrical

Power Requirements

Model FR-20	117 VAC $\pm 10\%$, 55-65 Hz (400 Hz optional), at approximately 7 watts
-------------	---

Model FR-10	7 VAC $\pm 10\%$ and 26 VAC $\pm 10\%$ center tapped, 55-65 Hz (400 Hz optional), obtained from equipment in which FR-10 is installed
-------------	---

Output Signals

- a. Composite sync
- b. Mixed blanking
- c. Horizontal (line) drive
- d. Vertical (field) drive

Each signal approximately 4 ± 0.5 volt (negative-going pulses) into a 75-ohm resistive load

Output Waveform

In accordance with EIA standards RS-170, RS-330, and RS-343.

Line/Frame Rates

As specified at time of purchase. Typical line rates are 525, 625, 875, 945, 1029, and 1225. Other line rates available.

TABLE 1-1
TECHNICAL SUMMARY (Cont'd)

Operating Modes	a. AFC locked to 60 Hz input power line frequency
	b. Free-running from internal solid state master oscillator
	c. Crystal-controlled (optional) from internal crystal oscillator
	d. External control (optional) from external square wave or pulse
Operating Stability	AFC lock in Range $\pm 4\%$
	AFC hold in Range $\pm 7\%$

Environmental

Operating Temperature Range	-20°C to 70°C (-4°F to +158°F)
Operating Humidity Range	Up to 95%

Mechanical

Dimensions (FR-20)	8-11/16 inches wide, 9-7/8 inches deep, 1-3/4 inches high
Weight (FR-20)	4 lbs
Mounting (FR-20)	Single rack mount, dual rack mount, or shelf mount
Signal Output Connectors (FR-20)	UHF coaxial type Goldline SO-239 or Amphenol 83-875

TABLE 1-2
OPTIONAL EQUIPMENT

Line Rate Kit	Kit consists of line rate jumper plug for selecting line rate of 525, 625, 675, 729, 735, 875, 945, 1029, 1203, 1225, 1329, or 1575. One line rate jumper plug is normally supplied as standard equipment. Line rate jumper plugs can be supplied for line rates other than those listed above.
Crystal Controlled Line Rate Kit	Kit consists of crystal and resistor (R24), and line rate jumper plug.
External Drive Kit (FR-20)	Consists of UHF coaxial connector (J21) type Goldline SO-239 or Amphenol 83-875, and a grounding ring terminal lug.
Rack Mounting Kits (FR-20)	See figure 2-3.

SECTION II

INSTALLATION

2-1. PRELIMINARY INSPECTION PROCEDURES

Upon delivery, check all items received against the packing slip enclosed. Follow the instructions for inspection and shipping damage procedure given in the damage claim procedure slip enclosed.

2-2. POWER REQUIREMENTS

The FR-10 Television Sync Signal Generator obtains its ac power from the Fairchild equipment in which it is installed.

The FR-20 Television Sync Signal Generator power requirement is 117 VAC $\pm 10\%$, 55-65 Hz (400 Hz optional), at approximately 7 watts. The power ON switch and a quarter-ampere fuse in the primary power circuit are located on the front panel.

Primary power is supplied to the FR-20 through a three-wire cable and three-pin grounding plug; a grounding plug to two-pin adapter with separate ground lead is included. The standard power cable is eight feet long and enters the unit through the rear panel.

2-3. FR-10 INSTALLATION

The FR-10 Television Sync Signal Generator is normally factory installed in Fairchild television equipment. The FR-10 signal and ac power terminals are either wired to the equipment wiring harness, or to a cable and plug that mates with a connector in the equipment. When the FR-10 is wired to a cable and plug, it is an option that is installed in the equipment at the factory.

2-4. FR-20 INSTALLATION

The Fairchild Television Sync Signal Generator Model FR-20 can be either shelf or rack mounted. Four uhf type output connectors marked VERT DRIVE, HOR DRIVE, BLANKING, and SYNC are located on the back of the chassis (see figure 2-1). Provision is made on the rear panel for installation of an optional external drive connector, J21. Provision is also made on the rear panel for another connector, J22, for use in special applications. All uhf type output connectors mate with type SO-239 connectors.



Figure 2-1. FR-20 Rear Panel

2-5. OUTLINE AND DIMENSIONS

See figure 2-2 for the outline and dimensions of the FR-20 Television Sync Signal Generator.

2-6. MOUNTING

The FR-20 may be desk or shelf mounted. It can be adapted to a standard 19-inch rack by using the kit shown in figure 2-3.

To rack mount the FR-20, use the following procedure:

1. Remove the top cover and base plate.
2. Remove the four screws that secure the front panel.
3. Using the front panel screws, and the kit screws supplied, attach the rack mounting kit to the FR-20 front panel, as shown in figure 2-3. Another similar unit may be mounted side by side with the FR-20 in place of the dummy panel.
4. Replace the top cover and base plate, but first turn both of them around, so that the front edges are at the rear of the unit; the cover and base plate will then fit flush behind the front panel.
5. When two units are mounted side by side, tie their rear panels together with the rear splice plate (not illustrated), to make a more rigid assembly.

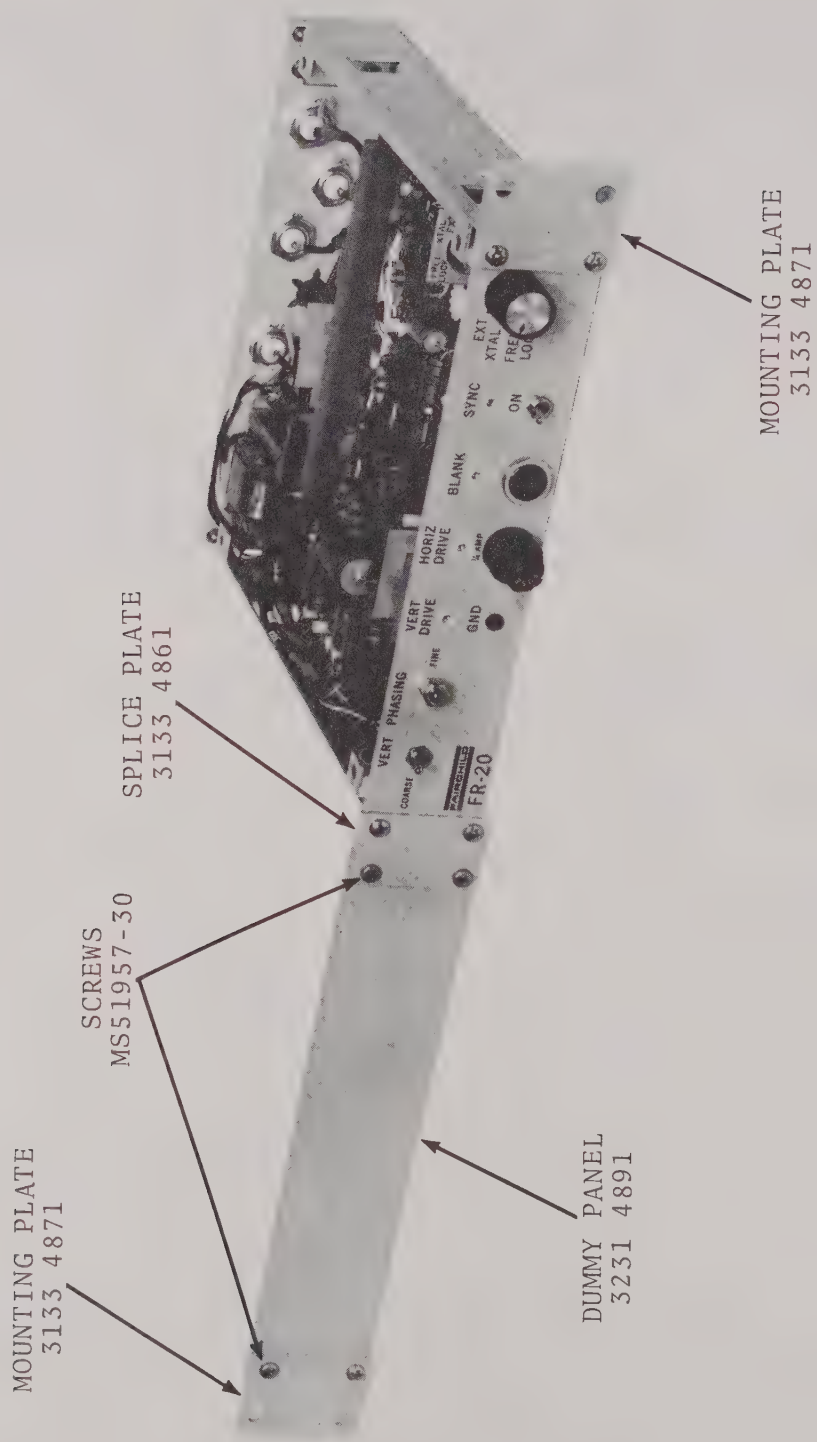


Figure 2-3. FR-20 Rack Mounting Kit

SECTION III

OPERATION

3-1. GENERAL

This section describes the front panel controls and test points, and provides procedures for the operation of the Fairchild Television Sync Signal Generator Model FR-20.

3-2. FRONT PANEL CONTROLS

Table 3-1 lists the location and function of all front panel controls and test points. The front panel is shown in figure 3-1.

3-3. OPERATION

Operate the sync generator as follows:

- a. Operate LOCK-FREE-XTAL-EXT switch to mode of operation desired.
- b. Operate power switch to ON.
- c. In the LOCK mode (in sync with the input ac power line frequency), the VERT PHASING controls will correct for cameras and viewer operating on different line phase inputs.

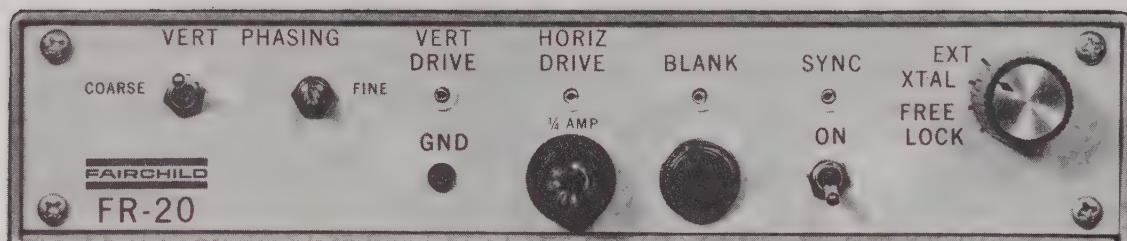


Figure 3-1. FR-20 Front Panel

TABLE 3-1
FRONT PANEL CONTROLS AND TEST POINTS

REF DES	NAME	FUNCTION
S1	LOCK-FREE-XTAL-EXT	LOCK position locks master oscillator into synchronism with ac power line frequency. FREE position permits master oscillator to run free. Optional XTAL position switches in crystal controlled oscillator when so equipped. Optional EXT position switches oscillator to external sync when so equipped.
S2	ON	Applies or removes ac line voltage.
S3	VERT PHASING COARSE	In the LOCK mode, changes the ac line input phase to the master oscillator afc circuit by 180 degrees.

TABLE 3-1

FRONT PANEL CONTROLS AND TEST POINTS (Cont'd)

REF DES	NAME	FUNCTION
R53	VERT PHASING FINE	In the LOCK mode, provides fine phase shift adjustment of ac power line reference frequency signal applied to the master oscillator afc circuit.
J12	VERT DRIVE	Test point for vertical drive output.
J13	HORIZ DRIVE	Test point for horizontal drive output.
J14	BLANK	Test point for mixed blanking output.
J15	SYNC	Test point for sync output.
J20	GND	Ground point for test purposes.
F1	1/4 AMP	Power line fuse.
DS1		Indicates that ac input power is ON.

SECTION IV THEORY

4-1. GENERAL

The following theory of operation applies to both the FR-10 and FR-20 Television Sync Signal Generators.

Basically, the sync generator consists of a master oscillator which generates a control frequency signal (clock), binary counter circuits which develop the vertical rate signal from the clock, circuits which develop blanking and sync signals, and afc circuits which sync the master oscillator to the ac power line frequency (see figures 4-1 and 4-2). These operate as follows:

4-2. MASTER OSCILLATOR

Master oscillator Z1 is an astable multivibrator with operating mode determined by LOCK-FREE-XTAL-EXT switch S1. When S1 is in the LOCK position, the master oscillator is maintained at the correct frequency by the afc circuit. In the FREE position of S1, the master oscillator is disconnected from the afc circuit and allowed to run free. Its natural frequency is adjusted by resistor R4. In the XTAL position of S1, the master oscillator is controlled by an optional quartz crystal unit (and associated resistor R24). In the EXT position of S1, the master oscillator is disabled and its output signal replaced by a signal from an external source, applied to optional connector J21.

When master oscillator Z1 is operating at the correct frequency, the output of the binary countdown chain at Z15 is at the correct 60-Hz field rate.

4-3. AFC CIRCUIT

The afc circuit consists of stages Q1, Q10, Q11, Q14, Q15 and diodes CR3, CR4, CR5, and CR6. The 60-Hz power line reference from the power supply is fed in through an RC filter network to afc amplifiers Q14 and Q15. At the bases of these stages the power line sine wave is given a dc component, adjustable with afc bias resistor R45, and then fed to a diode bridge formed by diodes CR3, CR4, CR5, and CR6. A 60-Hz sampling pulse is derived from the field pulse signal from 9-line flip-flop Z25 and fed through Q13 to afc paraphase amplifier Q12. The outputs of Q12 are fed to two ends of the diode bridge. The power line reference sine wave is sampled by the pulse outputs of Q12 and the instantaneous voltage value

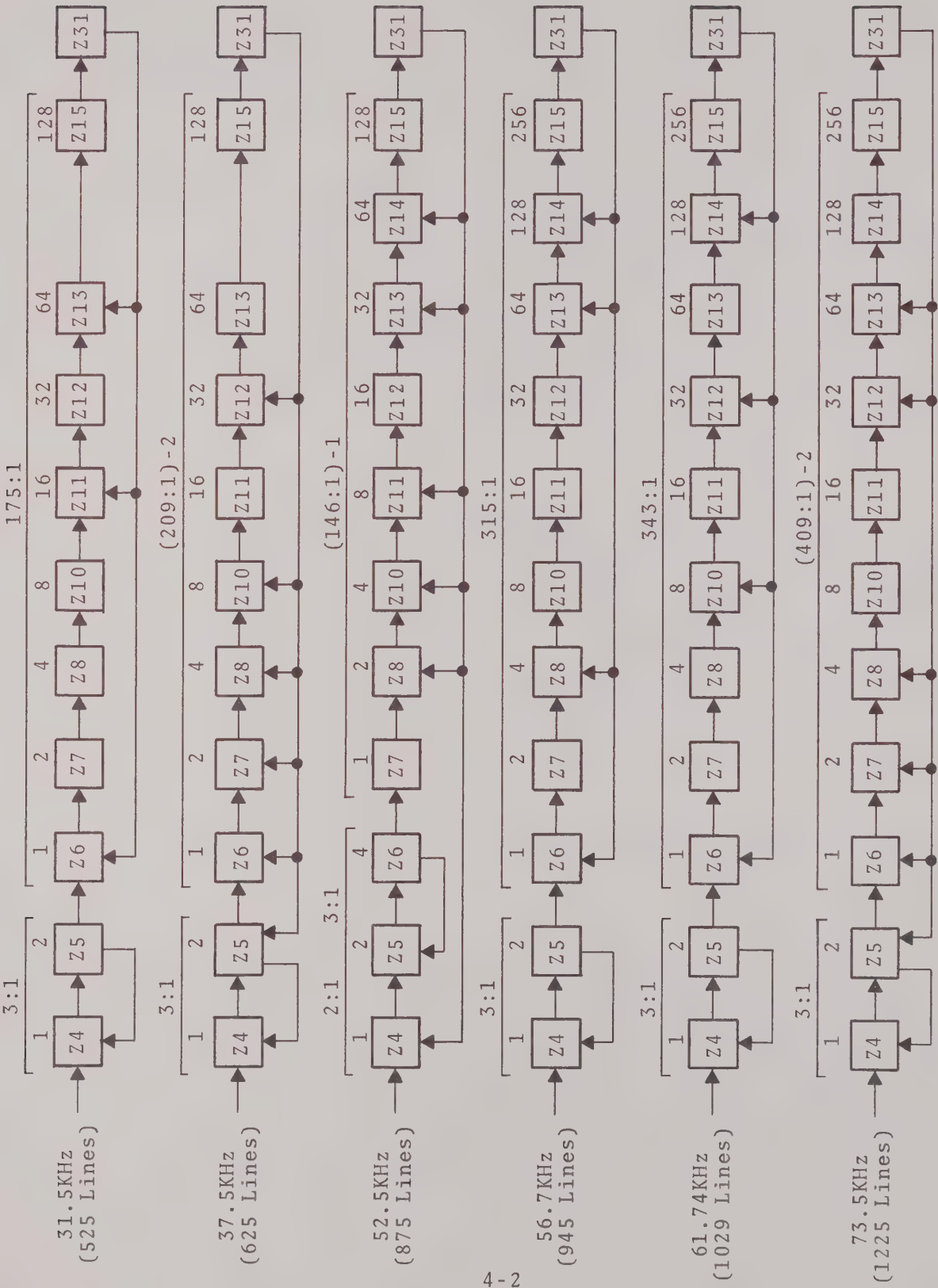


Figure 4-1. FR-10, FR-20 Television Sync Signal Generator, Counter Block Diagrams

of the sine wave is applied across capacitor C21. Since C21 cannot discharge rapidly between sampling pulses, dc voltage is generated, fed through afc amplifiers Q10 and Q11 and applied to switch S1A. When switch S1A is set to LOCK, this dc voltage is used to control the master oscillator frequency. Any tendency for the 60-Hz field pulse to drift with respect to the power line frequency causes the dc control voltage to change the frequency of the master oscillator to correct the drift.

In the FR-20 assembly, the 60-Hz power line reference sine wave is applied to the afc amplifiers Q14 and Q15 through an adjustable phase shift circuit. The phase shift circuit consists of COARSE phase adjustment switch S3, FINE phase adjustment R53, fixed capacitor C37, and fixed resistor R54. Switch S3 provides a complete phase reversal adjustment. Variable resistor R53 and capacitor C37 provide approximately 180 degrees of adjustable phase shift of the 60-Hz reference sine wave. The adjustments permit correction for cameras and viewers operating on different 60-Hz power line phase inputs.

4-4. COUNTDOWN CHAIN

The countdown chain consists of JK binary counters Z4 through Z8, and Z10 through Z15. The purpose of the countdown chain is to count the pulse output of the master oscillator (operating at twice the line rate frequency), and produce the 60-Hz vertical field rate pulse at its output at Z15. Outputs are also tapped off the countdown chain at the proper intervals for gating and triggering purposes.

Since the final output of a chain of binary counters is a power of two, it is necessary to modify the counter circuits to provide any count that is not a power of two. This count modification is accomplished by presetting some of the binary counters at the end of each count.

The preset pins of the binary counters are connected to pins on line rate jack J11. Some of the binary counters also have their complementary output pins connected to jack J11. The output of Z13, the input and output of Z14, and the input of Z15 are also connected to jack J11; this permits bypassing Z14, or jumpering it into the circuit, as required for proper countdown for the line rate in use. Differentiating capacitor C7 connects J11-29 to J11-30 which is connected to ground through resistor R29. J11-29 and J11-30 provide, through jumper connections in P11, the feedback pulses for modifying the counts of Z4 and Z5, or Z5 and Z6. Pins requiring ground connections are jumpered by P11 to J11-31.

The field rate output pulse of Z15 is applied to counter inverter amplifier Q18, whose output is differentiated,

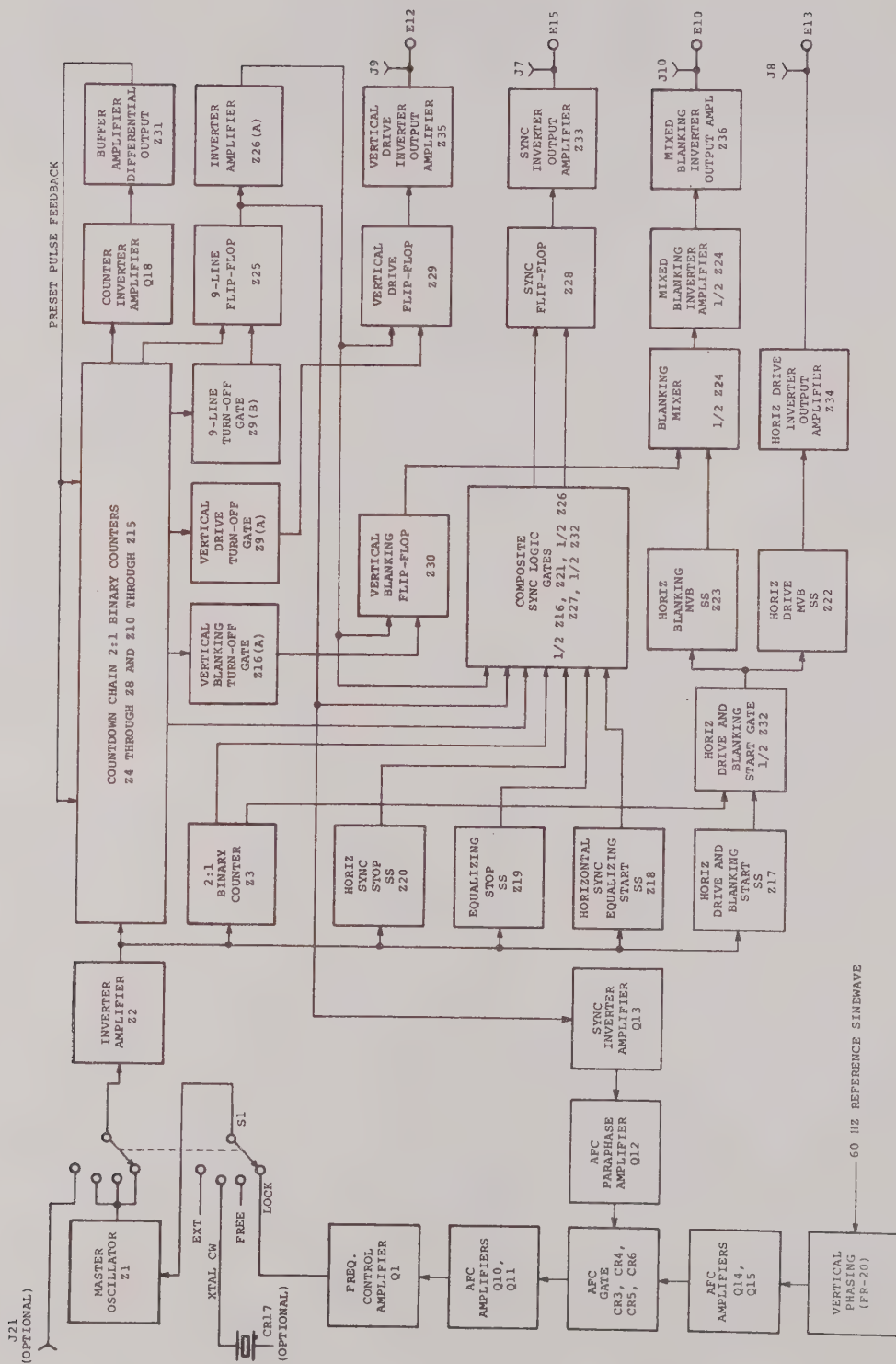


Figure 4-2. FR-10, FR-20 Television Sync Signal Generators, Simplified Block Diagram

amplified by buffer amplifier Z31 and applied as a positive trigger to pin 20 of jack J11. This positive trigger is connected by line rate jumper plug P11 to the proper pins of jack J11 to preset the proper countdown chain binaries for the line rate in use.

The complementary output of Z15 at pin 7 is differentiated by capacitor C9 and applied as a trigger to the 9-line flip-flop Z25 whose output at pin 6 goes from a positive level to ground. The complementary outputs of binaries Z7 and Z8 are connected to the inputs of 9-line turn-off gate Z9(B). At a count of 18 master oscillator pulses (9 lines), both inputs to Z9(B) go to ground resulting in a positive output of Z9(B), thereby resetting 9-line flip-flop Z25.

The output at pin 6 of the 9-line flip-flop Z25 is used as a gating signal in the composite sync generation circuit, applied to the afc circuit, and to the inverter amplifier Z26(A). The output of the inverter amplifier Z26(A) is used as a gating signal in the horizontal sync circuit and to trigger the vertical drive flip-flop Z29 and vertical blanking flip-flop Z30.

4-5. VERTICAL DRIVE AND VERTICAL BLANKING

The vertical drive flip-flop Z29 and vertical blanking flip-flop Z30 are triggered simultaneously by the positive pulse output of inverter amplifier Z26(A) which is driven by the output pulse of 9-line flip-flop Z25. Flip-flops Z29 and Z30 are reset by the positive pulse outputs of the vertical drive turn-off gate Z9(A) and vertical blanking turn-off gate Z16(A). The inputs to Z9(A) and Z16(A) are derived from the countdown chain by line rate jumper plug P11 which provides the proper reset timing for the line rate in use.

The vertical drive output of flip-flop Z29 is applied through vertical drive inverter output amplifier Z35 to E12 and test point jack J9. The vertical blanking output of flip-flop Z30 is applied to pin 2 of the blanking mixer half of Z24 and mixes with the output of horizontal blanking multivibrator Z23; the mixed blanking output is applied through the mixed blanking inverter amplifier half of Z24 to mixed blanking inverter output amplifier Z36. The output of Z36 is applied to terminal E10 and test point jack J10.

4-6. HORIZONTAL DRIVE AND BLANKING

The horizontal drive multivibrator Z22 and horizontal blanking multivibrator Z23 are single-shot multivibrators that are simultaneously triggered by the positive pulse output of the horizontal drive and blanking start gate Z32(B). One input

to Z32(B) is a trigger from the trailing edge of the output pulse of horizontal drive and blanking start single-shot Z17. Z17 is triggered at the master oscillator frequency by pulses from inverter amplifier Z2, and its output pulse width is adjustable. The other input to Z32(B) is a gating pulse from 2:1 binary counter Z3 which also receives a signal at the master oscillator frequency from inverter amplifier Z2. The pulse from binary counter Z3 inhibits every other trigger from Z17, resulting in output triggers from Z32(B) at the horizontal line rate, which are then applied to horizontal drive multivibrator Z22 and to the horizontal blanking multivibrator Z23. The adjustable width output pulse of Z22 is applied through horizontal drive inverter output amplifier Z34 to terminal E13 and horizontal drive test point jack J8.

The adjustable width output pulse of Z23 is applied to the blanking mixer half of Z24 and mixed with the vertical blanking. The mixed blanking output is fed through the mixed blanking inverter amplifier half of Z24 to mixed blanking inverter output amplifier Z36. The output of Z36 is applied to terminal E10 and to mixed blanking test point jack J10.

4-7. COMPOSITE SYNC CIRCUIT

The composite sync signal is generated by sync flip-flop Z28 which is set and reset by triggers derived from the master oscillator and from single shots triggered by the master oscillator.

The pulses from the master oscillator are applied at E22 to inverter amplifier Z2. The output of Z2 is applied to 2:1 binary counter Z3, horizontal sync start single-shot Z18, equalizing stop single-shot Z19, and to sync stop single-shot Z20. Pulses from master oscillator Z1 are fed to one of the inputs to serration start gate Z16(B). The 2:1 binary counter Z3 output pulses are at the horizontal line rate and are used for gating. The outputs of single-shot Z18 to Z21 are adjustable width pulses which are differentiated, with trailing edge spikes used as start and stop triggers which are gated to the sync flip-flop Z28.

From the start of the countdown until the generation of the vertical rate field pulse, the following conditions exist in the composite sync generation circuit:

The output at pin 6 of 9-line flip-flop Z25 is at a positive level and is applied to one of the inputs of the serration start gate Z16(B), to one of the inputs of equalizing stop gate Z27(B), and to inverter amplifier Z26(A). Serration start gate Z16(B) and equalizing stop gate Z27(B) are both disabled, preventing triggers from master oscillator Z1 and equalizing



stop single-shot Z19 from reaching sync flip-flop Z28. The output of inverter amplifier Z26(A) is at ground and enables the sync start gate/gate Z21(A) and sync stop gate Z26(B). Sync start gate/gate Z21(A) allows inhibit pulses from the 2:1 binary counter Z3 to pass through to sync start gate Z21(B) to inhibit every other trigger received from the horizontal sync and equalizing start single-shot Z18. The output triggers from Z21(B) at pin 6 are start triggers at the horizontal line rate and are applied to sync flip-flop Z28. Triggers from the horizontal sync stop single-shot Z20 at the master oscillator rate pass through the sync stop gates Z26(B) and Z27(A) to inverter amplifier Z32(A). The output of Z32(A) resets sync flip-flop Z28. The output of Z28 is a train of pulses (positive) at the horizontal line rate; the pulse width is determined by the adjustments of single-shots Z18 and Z20. The output of Z28 is applied through the sync inverter output amplifier Z33 to terminal E15 and sync test point jack J7.

At the completion of the countdown, the vertical field rate pulse generated at pin 7 of binary counter Z15 changes the state of 9-line flip-flop Z25. The output of Z25 at pin 6 goes from positive level to ground. This output is applied to inverter amplifier Z26(A), whose positive level output disables sync start gate/gate Z21(A) and also disables sync stop gate Z26(B). As a result, the inhibit pulses from the 2:1 binary counter Z3 are removed from the input to sync start gate Z21(B), and allow all the triggers from horizontal sync and equalizing start single-shot Z18 to be applied to sync flip-flop Z28. Thus Z28 is triggered at twice the horizontal line rate. The change of the output of 9-line flip-flop Z25 from positive to ground also removes one of two disabling signals from equalizing stop gate Z27(B), and from serration start gate Z16(B). The other switching input to Z27(B) is from pin 5 of countdown chain binary Z7, and is at ground for the first three and last three lines of the 9-line period. Z27(B) is enabled, and stop triggers from equalizing stop single-shot Z19, at twice the line rate, are applied through sync stop gate Z27(B), and inverter amplifier Z32(A) to sync flip-flop Z28. Thus Z28 generates the two groups of equalizing pulses; pulse width is determined by the adjustments of single-shots Z18 and Z19.

At the end of the first three lines of the 9-line period, countdown binary Z7 changes state. The output of Z7 at pin 5 goes to a positive level and disables equalizing stop gate Z27(B). The output of pin 7 of Z7 goes from a positive level to ground and enables serration start gate Z16(B). Master oscillator pulses from capacitor C5 pass through serration start gate Z16(B), sync stop gate Z27(A), and inverter amplifier Z32(A) to sync flip-flop Z28. Thus Z28 generates the serrated pulse for vertical sync. At the end of the second 3-line period, countdown binary Z7 changes state; the serration start gate is disabled, the equalizing stop gate is enabled, and the second group of equalizing pulses is generated.

SECTION V

ADJUSTMENTS & MAINTENANCE

5-1. ADJUSTMENTS

All the following adjustments are performed internally. Test points are located on the front panel and internally in the sync generator. Table 5-1 lists the recommended test equipment required. Waveforms, test points, adjustment designations and locations are shown in this section (see figures 5-1 through 5-11). Refer to figure 6-2 (sheets 1 of 2, and 2 of 2) schematics for use in troubleshooting.

TABLE 5-1. RECOMMENDED TEST EQUIPMENT

Test Equipment	Manufacturer	Function and Description
Oscilloscope Type 766H with Type 76-02A Dual Trace Plug-In, Type 74-13A Time Base Plug-In, and 10:1 Probe	Fairchild	Monitors waveforms; oscilloscope should meet following minimum requirements: Vertical Sensitivity 0.005 volt per centimeter Time Base 0.01 usec to 0.10 sec full scale Bandwidth 25 Hz
Multimeter Model 260	Simpson	Measures ac volts, dc volts, and resistance.
Output Terminations		UHF Coaxial Four connectors with 75-ohm terminating resistors

5-2. ADJUSTMENT AND TEST SETUP

Terminate FR-10 or FR-20 Television Sync Signal Generator signal outputs with 75-ohm loads before making adjustments and observing waveforms.

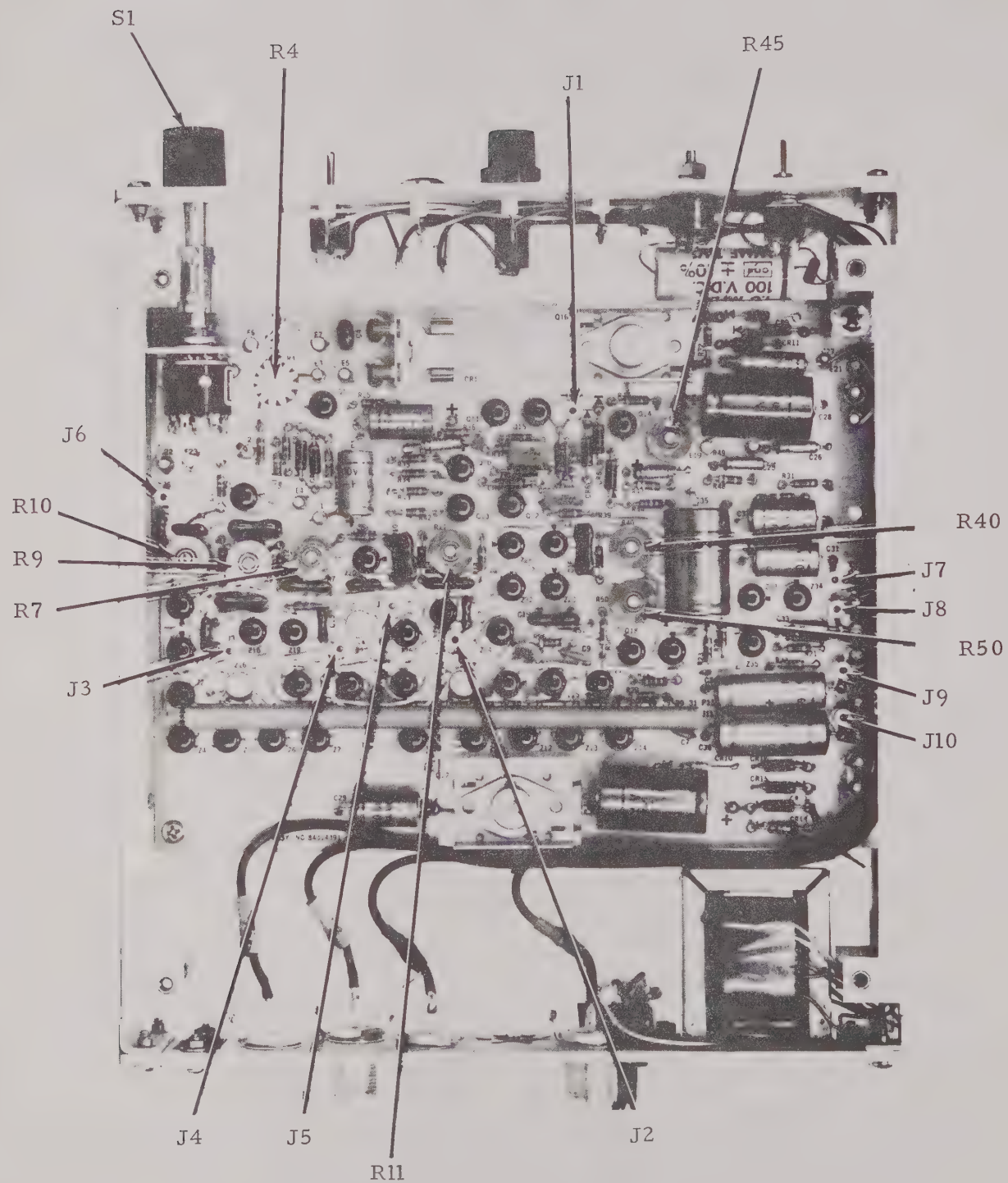
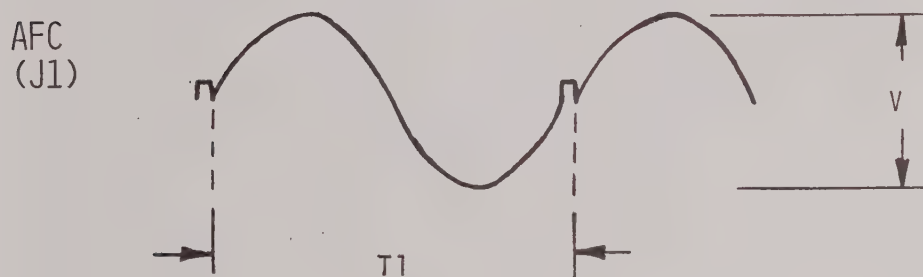


Figure 5-1. FR-10, FR-20 Television Sync Signal Generator, Test Points and Adjustments

5-3. AFC AND MASTER OSCILLATOR ADJUSTMENTS

- a. Observe waveform at 60-Hz rate at J1 with oscilloscope locked to 60-Hz input line frequency (see figure 5-2). On the FR-20, set FINE phase control R53 fully CCW.
- b. Place LOCK-FREE-XTAL-EXT switch (S1) to FREE position. Adjust the frequency adjustment R4 until the notch in the signal stops its free-running movement.
- c. Place LOCK-FREE-XTAL-EXT switch to LOCK. The notch signal should be in sync on the oscilloscope.
- d. Adjust AFC Bias R45 (same setting for all line rates) until the notch is in the center of the signal.



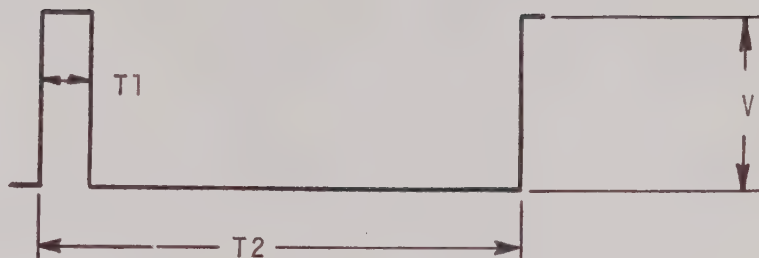
LINE RATE	525	625	875	945	1029	1225
V (VOLTS)	4 ±1V					
T1 (MSEC)	16.66	16.66	16.66	16.66	16.66	16.66
Adjustment	FREQ ADJ R4 and AFC BIAS - R45					
Oscilloscope Synchronization	From 60-Hz Power Line Frequency On the FR-20 set FINE phase control R53 fully CCW					

Figure 5-2. AFC and Master Oscillator Adjustment and Waveform.

5-4. ADJUSTMENT OF HORIZONTAL SIGNALS

The following illustrations and charts (see figures 5-3 through 5-13) show location of waveform test points and adjustments for the horizontal pulse widths. The charts indicate waveforms and setting for various line rates and the synchronizing signal source for the oscilloscope.

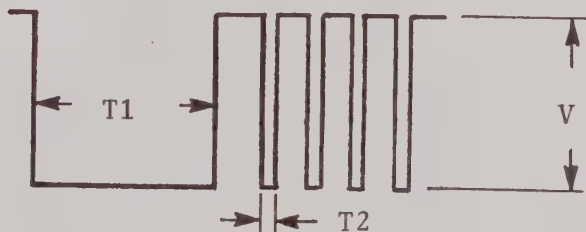
HOR DRIVE
& BLK START
(J2)



LINE RATE	525	625	875	945	1029	1225
V (VOLTS)	1.5					
T1 (USEC)	3.0	2.5	1.8	1.7	1.5	1.3
T2 (USEC)	31.75	26.75	19.0	17.6	16.2	13.6
Adjustment	Horizontal Drive and Blanking Start - R11					
Oscilloscope Synchronization	From Master Oscillator - J6					

Figure 5-3. Horizontal Drive and Blanking Start, Adjustment and Waveform.

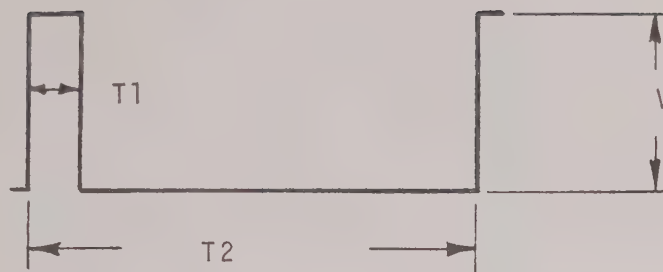
MIXED
BLANKING
(J10)



LINE RATE	525	625	875	945	1029	1225
V (VOLTS)	4.0					
T1 (USEC)	1100 TO 1400					
T2 (USEC)	11.0	8.6	6.5	6.0	5.6	4.0
Adjustment	Horizontal Blanking Width - R50					
Oscilloscope Synchronization	From Vertical Drive at Test point J9 - T1 From Horizontal Drive and Blanking Start Test Point J2 - T2					

Figure 5-4. Horizontal Blanking Width Adjustment and Waveform.

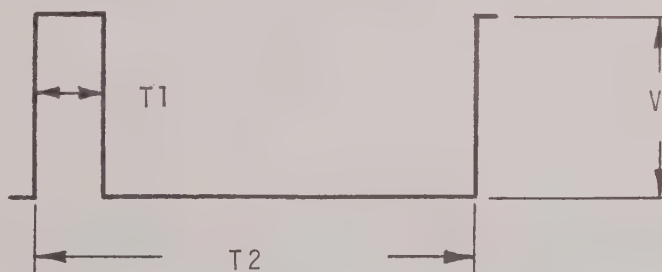
HOR SYNC
& EQ START
(J3)



LINE RATE	525	625	875	945	1029	1225
V (VOLTS)	1.5					
T1 (USEC)	4.4	3.4	2.6	2.4	2.2	1.87
T2 (USEC)	31.75	26.75	19.0	17.6	16.2	13.6
Adjustment	Horizontal Sync and Equalizing Start - R10					
Oscilloscope Synchronization	From Master Oscillator - J6					

Figure 5-5. Horizontal Synchronizing and Equalizing Start, Adjustment and Waveform.

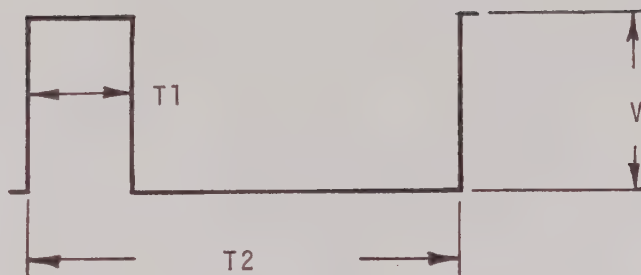
EQ STOP
(J4)



LINE RATE	525	625	875	945	1029	1225
V (VOLTS)	1.5					
T1 (USEC)	6.7	5.2	4.0	3.7	3.4	2.9
T2 (USEC)	31.75	26.25	19.0	17.6	16.2	13.6
Adjustment	Equalizing Stop - R9					
Oscilloscope Synchronization	From Master Oscillator - J6					

Figure 5-6. Equalizing Stop, Adjustment and Waveform.

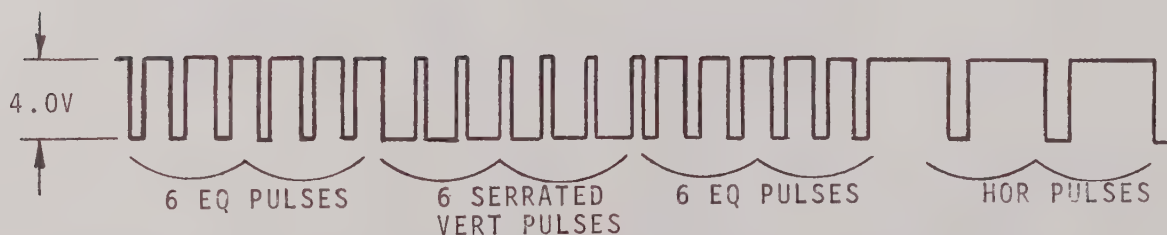
HOR SYNC
STOP
(J5)



LINE RATE	525	625	875	945	1029	1225
V (VOLTS)	1.5					
T1 (USEC)	9.1	7.1	5.5	5.0	4.65	3.9
T2 (USEC)	31.75	26.75	19.0	17.6	16.2	13.6
Adjustment	Horizontal Synchronizing Stop - R7					
Oscilloscope Synchronization	From Master Oscillator - J6					

Figure 5-7. Horizontal Synchronizing Stop, Adjustment and Waveform.

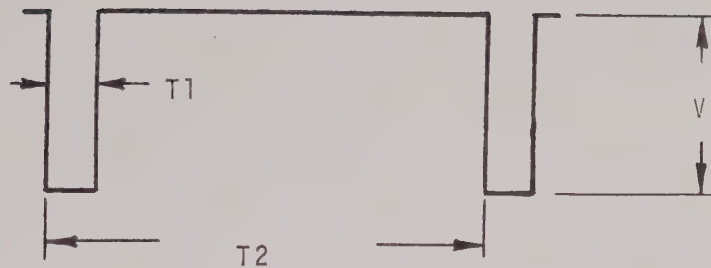
SYNC
(J7)



Oscilloscope Synchronization	From Vertical Drive J9 (Set Oscilloscope Mode Switch to ALTERNATE).
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Figure 5-8. Synchronization Waveform.

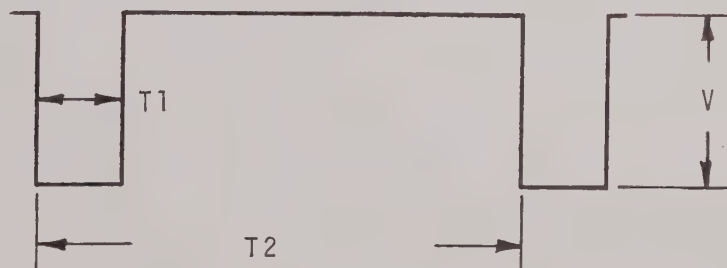
HOR DR
(J8)



LINE RATE	525	625	875	945	1029	1225
V (VOLTS)	4.0					
T1 (USEC)	6.3	4.9	3.8	3.5	3.2	2.7
T2 (USEC)	63.5	49.5	38.0	35.2	32.5	27.2
Adjustment	Horizontal Drive - R40					
Oscilloscope Synchronization	From Horizontal Drive/Blanking Start - J2					

Figure 5-9. Horizontal Drive, Adjustment and Waveform.

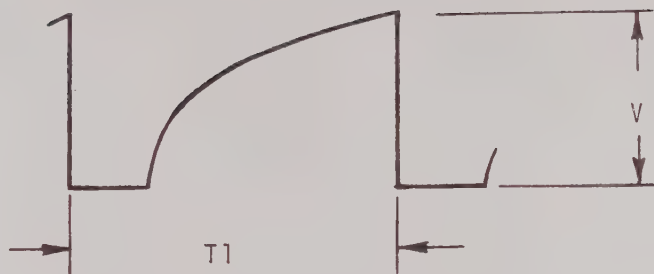
VERT DR
(J9)



LINE RATE	ALL
V (VOLTS)	4.0
T1 (USEC)	570 TO 762
T2 (MSEC)	16.66
Adjustment	None

Figure 5-10. Vertical Drive, Waveform.

MASTER OSC
Z1 PIN 7
(J6)



LINE RATE	525	625	875	945	1029	1225
V (VOLTS)	3.0					
T1 (USEC)	31.75	26.65	19.0	17.6	16.2	13.6
Oscilloscope Synchronization	From Master Oscillator - J6					

Figure 5-11. Master Oscillator Z1,
Pin 7 Waveform.

5-5. MAINTENANCE

5-6. GENERAL. The pin numbers of all micrologic units are read clockwise when looking at the pin side of the device. On the T0-5 metal can type micrologic, the first pin clockwise of the tab is pin 1. On the epoxy case type micrologic, the first pin clockwise of the white dot or small "flat" on the side of the case is pin 1. The tab, white dot, or small "flat", locates pin 8 or pin 10, depending on whether an 8-pin or a 10-pin micrologic is used. If a pin is not used on a micrologic the pin space for it is counted nevertheless. The micrologics are identified by their reference designations, which are stencilled on the component side of the component board. A stencilled arrow head identifies the location of pin 8 of an 8-pin micrologic socket, or pin 10 of a 10-pin micrologic socket.

On the solder side of the component board the micrologic pins can be identified by referring to the schematic diagram, figure 6-2, and noting the connections of the schematic diagram and of the component board printed circuit. Pin 8 of 8-pin micrologics, and pin 10 of 10-pin micrologics are connected to B+. The B+ used for the micrologics is +3.6 volts regulated, except for Sync Flip-Flop Z28, the four Inverter Output Amplifiers Z33 through Z36, and Master Oscillator Z1, which all use +8.4 volts regulated.

A more detailed description of the micrologics used in the FR-10 and FR-20 is given in Appendix A, Logic and Logic Circuits.

5-7. TROUBLESHOOTING. The Theory of operation, Section IV, the adjustment and troubleshooting waveforms, the voltage and resistance tables, and the schematic diagrams are provided to aid troubleshooting.

CAUTION

1. Do not perform resistance measurements on micrologic circuits. The comparatively high voltage from the ohm-meter may damage the circuits.
2. Do not adjust variable resistors at random. If it is necessary to change the setting of a variable resistor for a test, note the original setting of the resistor. Return the resistor to the original setting, before proceeding to other tests.
3. When troubleshooting a circuit with the aid of a large bypass capacitor, completely discharge the capacitor before each test. Otherwise, the residual charge in the capacitor may be great enough to exceed the current ratings of the transistors and micrologic elements in the circuit being tested.

NOTE

All the outputs must each be terminated with a 75-ohm load, when output waveforms are being checked.

If the FR-10 or FR-20 does not appear to function correctly, initially perform the following steps:

1. Verify the setting of LOCK-FREE-XTAL-EXT switch S1.
2. If all outputs are absent, check for +3.6 vdc regulated at the positive side of C29, and for +8.4 vdc regulated at the emitter of Voltage Regulator Q16 (this voltage can be conveniently measured at the end of R31 furthest from the edge of the component board; the other end of R31 is at +3.9 vdc zener). R31 is located between large capacitor C28 and C32. If both these voltages are absent, check the equipment fuse, ac line power input, and power supply circuit.
3. If all the outputs are present but incorrect, check the master oscillator, which is the basic timing source of the unit. Put LOCK-FREE-XTAL-EXT switch S1 in the FREE position, and check the waveform, figure 5-11 and 5-14, at Master

Oscillator Period test point jack J6, figure 5-1. An incorrect indication at J6 indicates a defective Z1 or Q1 stage. If the waveform at J6 is correct, check the output waveform at Inverter Amplifier Z2 pin 5, figure 5-14, to isolate a possible Z2 defect.

4. Check the afc lock-in circuit by checking for a reference sinewave at terminal E21. Check for sampling pulses at the emitter and collector of Afc Paraphase Amplifier Q12 (figure 5-13, sheet 1).

NOTE

If repairs are required in the afc circuits, readjust the frequency adjustment R4, and Afc Bias adjustment R45, as described in paragraph 5-3.

5. If some of the outputs are present and correct, and some are absent or present and incorrect, refer to the simplified block diagram, figure 4-2, to isolate possible trouble to a particular circuit.

6. If an incorrect count in the countdown chain is suspected, check that preset pulses are being fed to the countdown chain binary pins on jack J11. The preset pulse pins for each line rate are listed in Note 6 on figure 6-2, sheet 1. Also refer to figure 4-1. If all preset pulses are absent, trace back from J11 pin 20 through Z31, Q18, to Z15 pin 5, to isolate a defective stage. If some preset pulses are present and some absent, check line rate jumper plug P11.

7. If all the preset pulses are present, and an incorrect count is evident, trace the count stage by stage through the countdown chain, from input to output, to isolate a defective binary stage. Note, however, that 9-Line Turn-off Gate Z9(B) provides a positive output at a count of 18 master oscillator pulses (9 lines), and may be used as a check up to the output of binary Z8.

5-8. REPAIR. In general, replace parts in the FR-10 or FR-20 using the same techniques as used for any other transistorized electronic equipment; however, when replacing transistors or micrologic elements, use the lowest wattage soldering iron compatible with the task.

When replacing micrologics and transistors, it is recommended that only the exact replacement be used to assure proper operation.

Most micrologic elements can be replaced without any readjustment, except when replacing a micrologic in a multivibrator stage. Then, the multivibrator should be readjusted for its proper pulse width.

5-9. VOLTAGE TABLE

Table 5-2 lists nominal voltage measurements of a normally functioning FR-10 or FR-20 Sync Generator, operating at a 525 line rate.

Voltages are measured to ground, and are positive and dc unless otherwise stated.

Signal outputs are each terminated with a 75-ohm load for voltage measurements.

Ac line power input is 115 vac, 60 Hz.

TABLE 5-2. TRANSISTOR VOLTAGES

CIRCUIT	EMITTER	BASE	COLLECTOR
+8.4 vdc Regulator Q16	+7.6 to +9.2	+9.1 zener	+17
+3.6 vdc Regulator Q17	+3.2 to +4.0	+3.9 zener	+7.2
Frequency Control Amplifier Q1	+3.8	+3.2	0
AFC Amplifier Q10	+2.8	+3.4	+6.5
AFC Amplifier Q11	+3.4	+2.8	+6.5
AFC Paraphase Amplifier Q12	+0.15 (60-Hz pulse)	+0.2 (60-Hz pulse)	+7.8 (60-Hz pulse)
Sync Inverter Amplifier Q13	0 (ground)	+0.6 (60-Hz pulse)	+0.2 (60-Hz pulse)
AFC Amplifier Q14	+4.0 (60-Hz sinewave)	+4.4 (60-Hz sinewave)	+8.4 regulated
AFC Amplifier Q15	+4.0 (60-Hz sinewave)	+3.5 (60-Hz sinewave)	0 (ground)
Counter Inverter Amplifier Q18	0 (ground)	+0.3 (60-Hz pulse)	+2.8 (60-Hz pulse)

5-10. RESISTANCE TABLES

Resistances listed in the following tables are measured to ground, unless otherwise stated. The common lead (negative) of the multimeter is connected to ground, unless otherwise stated. Signal outputs are not terminated for resistance measurements. Resistances are in ohms, K = thousands, M = millions. Before making each resistance measurement, set the multimeter to the range indicated in parenthesis for each resistance to be measured.

CAUTION

Disconnect power cable plug from the 115 vac supply before making resistance measurements.

TABLE 5-3. TRANSISTOR RESISTANCES

CIRCUIT	EMITTER	BASE	COLLECTOR
+8.4 vdc Regulator Q16*	950 (X 100)	2.8K (X 100)	2.8K (X 100)
+3.6 vdc Regulator Q17*	600 (X 100)	1.1K (X 100)	80K (X 10,000)
Frequency Control Amplifier Q1*	50 (X1)	1.8K (X 100)	0 (X1)
AFC Amplifier Q10*	1.5K (X 100)	3K (X 100)	2.4K (X 100)
AFC Amplifier Q11*	3.2K (X 100)	6K (X 100)	2.4K (X 100)
AFC Paraphase Amplifier Q12*	1K (X 100)	2.4K (X 100)	2.2K (X 100)
Sync Inverter Amplifier Q13*	0 (X1)	17 (X1)	2.4K (X 100)
AFC Amplifier Q14*	1K (X 100)	4K (X 100)	950 (X 100)
AFC Amplifier Q15*	1K (X 100)	7K (X 100)	0 (X1)
Counter Inverter Amplifier Q18*	0 (X1)	17 (X1)	1.5K (X 100)

*Set multimeter to range shown in parenthesis.

TABLE 5-4. COMPONENT BOARD TERMINAL RESISTANCES

TERMINAL	RESISTANCE TO GROUND
E8	100K Approx. (X 10,000)
E9	100K Approx. (X 10,000)
E10	30K (X 10,000)
E11	0 (X 1)
E12	50K Approx. (X 10,000)
E13	90K (X 10,000)
E14	0 (X 1)
E15	50K (X 10,000)
E16	0 (X 1)
E17	18K (X 10,000)
E18	18K (X 10,000)

NOTE

Terminal resistances measured with no external circuitry connected to component board. Set multimeter to range shown in parenthesis.

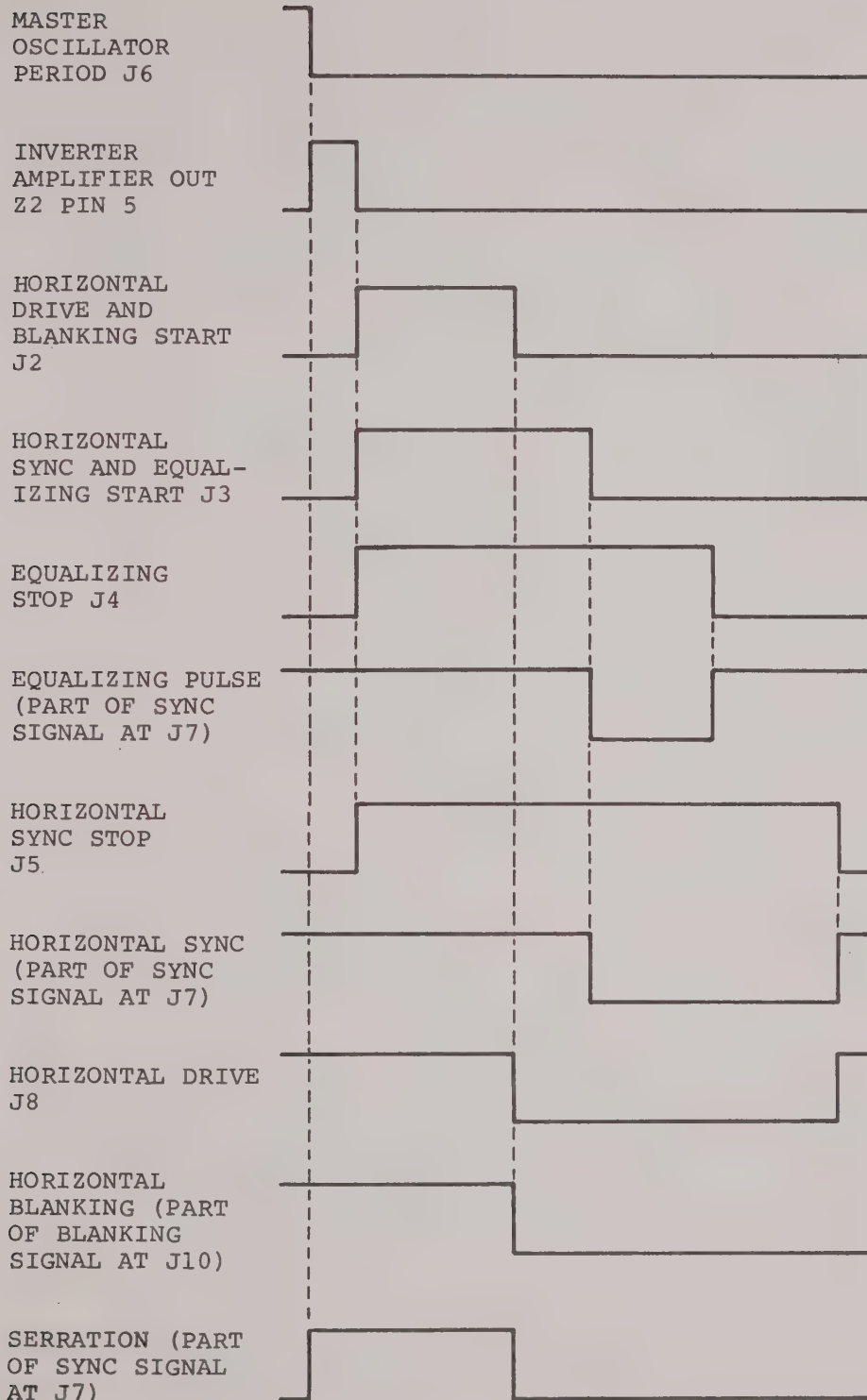
TABLE 5-5. FR-20 POWER TRANSFORMER WINDING RESISTANCES

WINDING	RESISTANCE	REMARKS
Primary	68 Approx. (X 1)	Measured at Pins of Power Cable Plug
26 vac Center-tap	4 Approx. either side of Center-tap. (X 1)	
7 vac	1.5 Approx. (X 1)	

5-11. TROUBLESHOOTING WAVEFORMS

Figure 5-12 is a Master Timing Chart that shows the timing relationship of some of the waveforms. Figures 5-13 through 5-22 show typical waveforms for a line rate of 525. Pulse amplitudes are nominal and may vary for different line rates, and from one micrologic to another.

The signal outputs must each be terminated in a 75-ohm load.



NOTE: Pulse widths are determined by the line rate. See waveforms in Figures 5-2 through 5-11 for exact width and amplitude for a particular line rate.

Figure 5-12. Master Timing Chart FR-10, FR-20

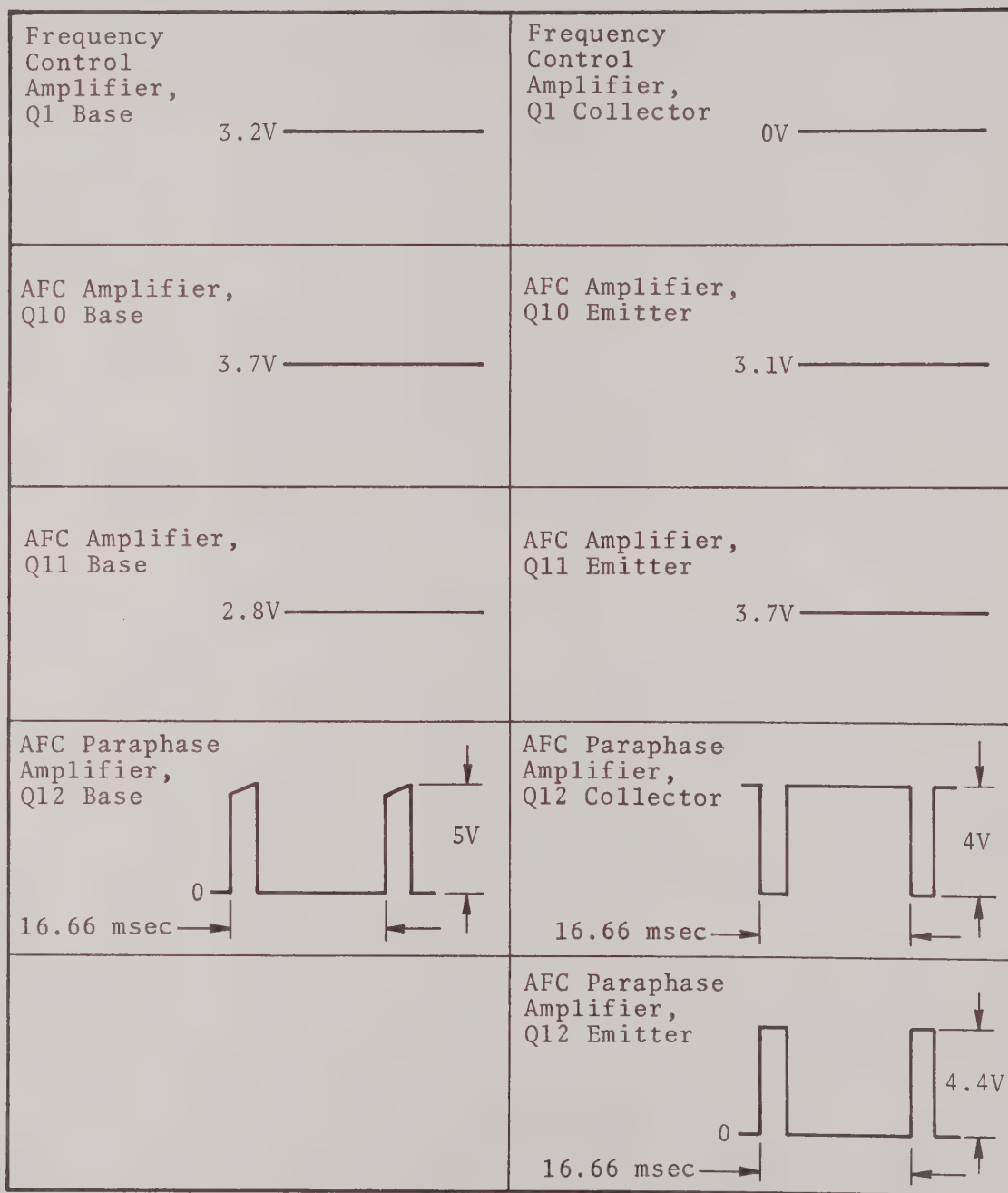


Figure 5-13. FR-10, FR-20 Transistor Waveforms (Sheet 1 of 2)

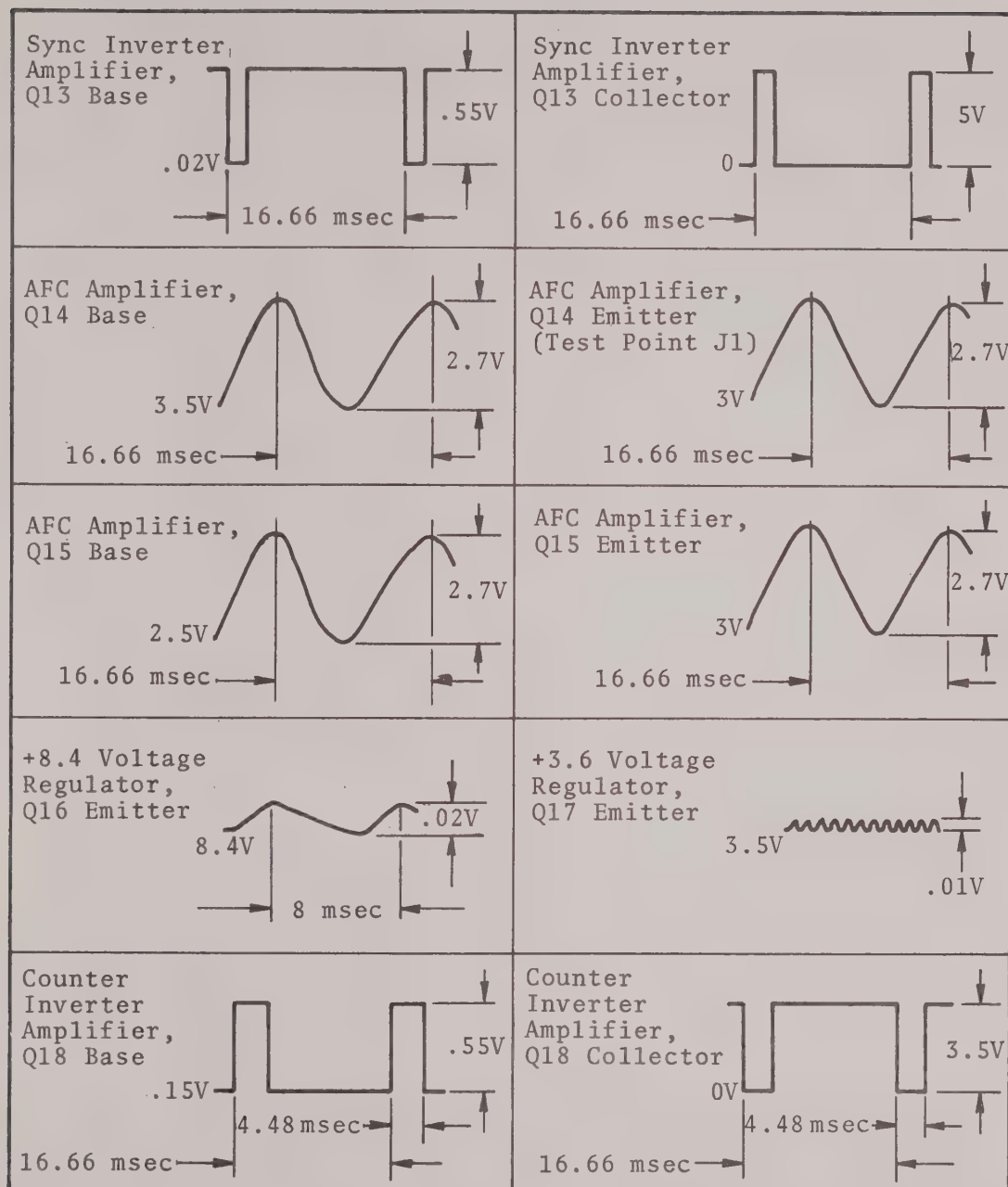
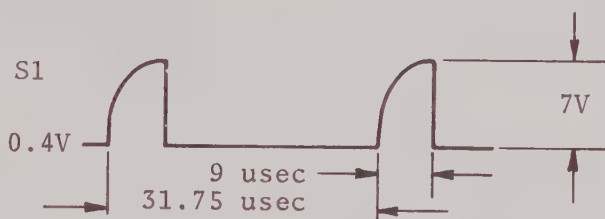


Figure 5-13. FR-10, FR-20 Transistor Waveforms (Sheet 2 of 2)

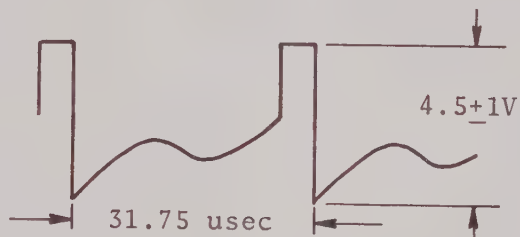
Master Oscillator Input,
Z1 pin 1
Lock/Free/Xtal/Ext Switch S1
in FREE position.



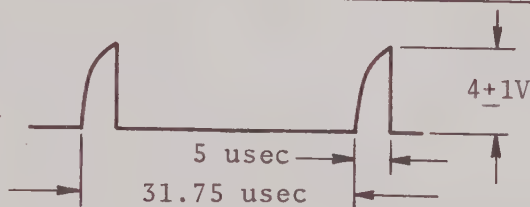
Master Oscillator Output,
Z1 pin 7 (Test Point J6)
Lock/Free/Xtal/Ext Switch S1
in FREE position.
Frequency Control R4
Adjustment Range 15
to 34 usec.



Master Oscillator Input,
Z1 pin 3 (Terminal E7)
Lock/Free/Xtal/Ext Switch S1
in XTAL position, and Crystal
Unit CR17 and Resistor R24
installed.



Master Oscillator Output,
Z1 pin 7 (Test Point J6)
Lock/Free/Xtal/Ext Switch S1
in XTAL position, and Crystal
Unit CR17 and Resistor R24
installed.



Inverter Amplifier Input,
Z2 pin 3



Inverter Amplifier Output,
Z2 pin 5

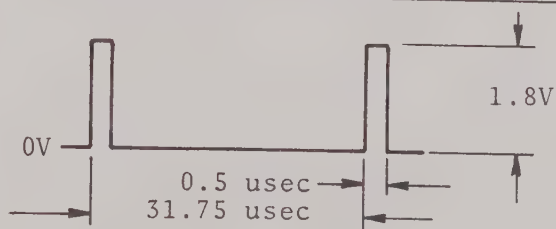


Figure 5-14. FR-10, FR-20 Master Oscillator Z1 and Inverter Amplifier Z2 Waveforms, 525 Line Rate

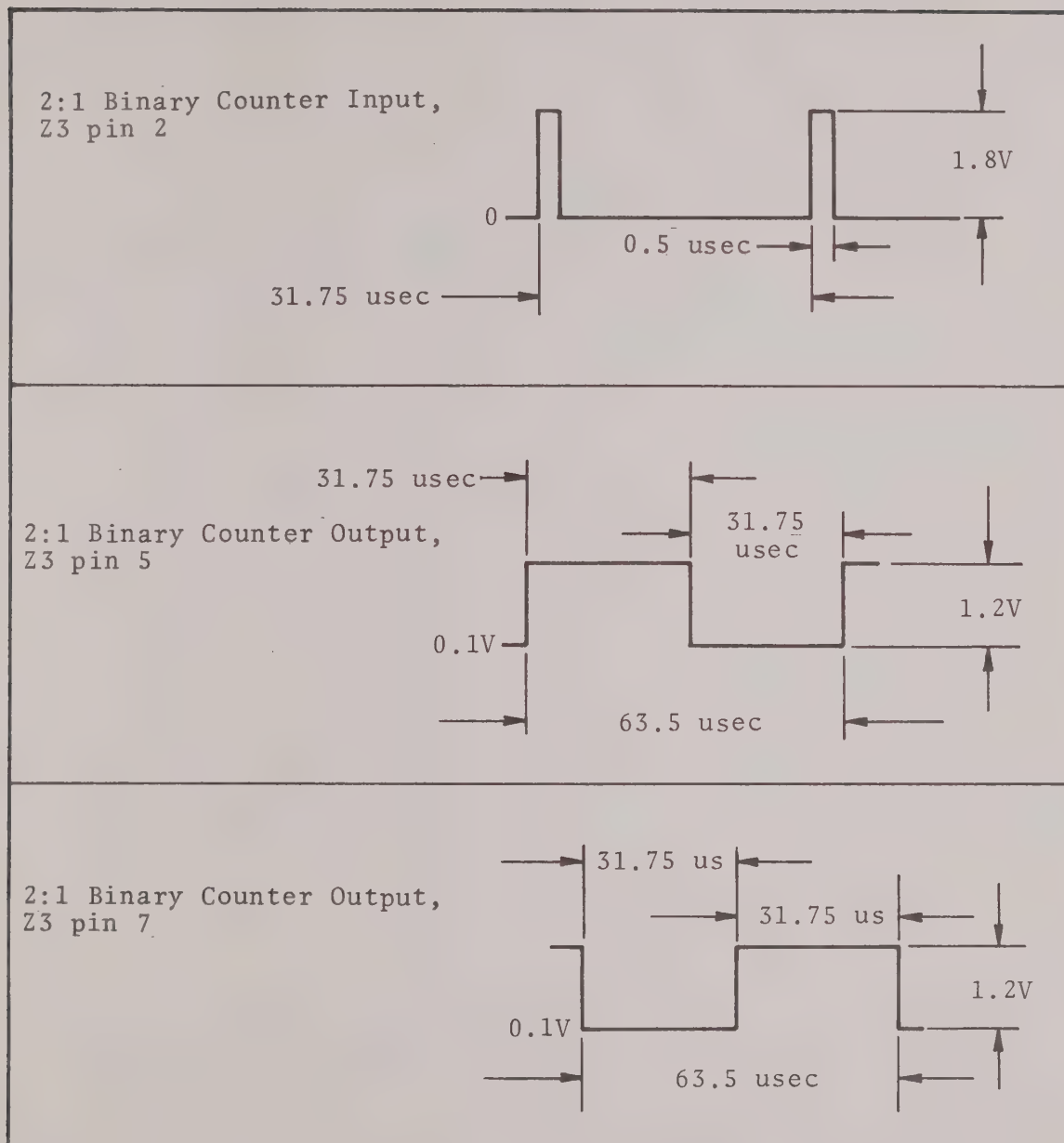
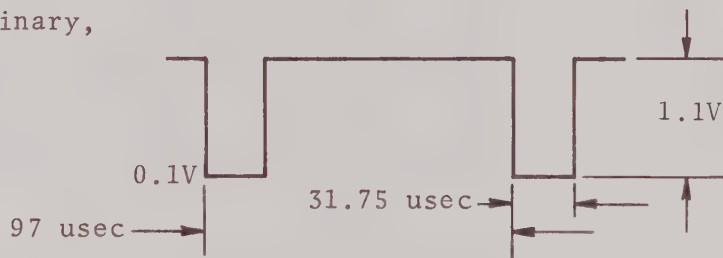


Figure 5-15. FR-10, FR-20 2:1 Binary Counter Z3 Waveforms,
525 Line Rate.

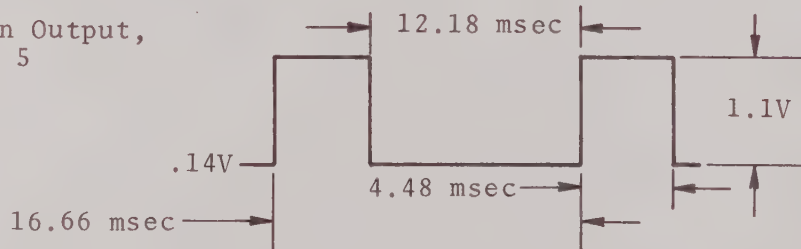
Countdown Chain Input
Binary, Z4 pin 2
(3:1 Count Input)



3:1 Count Output Binary,
Z5 pin 5



Countdown Chain Output,
Binary Z15 pin 5
(Preset Pulse)



Countdown Chain Output,
Binary Z15 pin 7
(Vertical Field Rate Pulse)

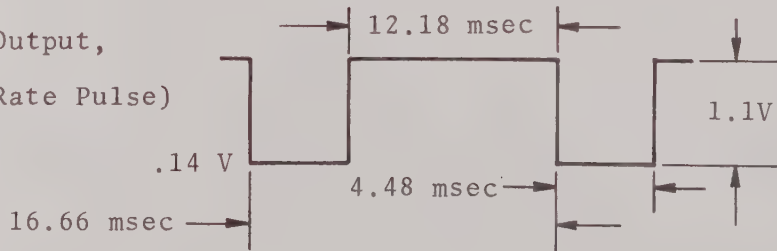


Figure 5-16. FR-10, FR-20 Countdown Chain Waveforms,
525 Line Rate.

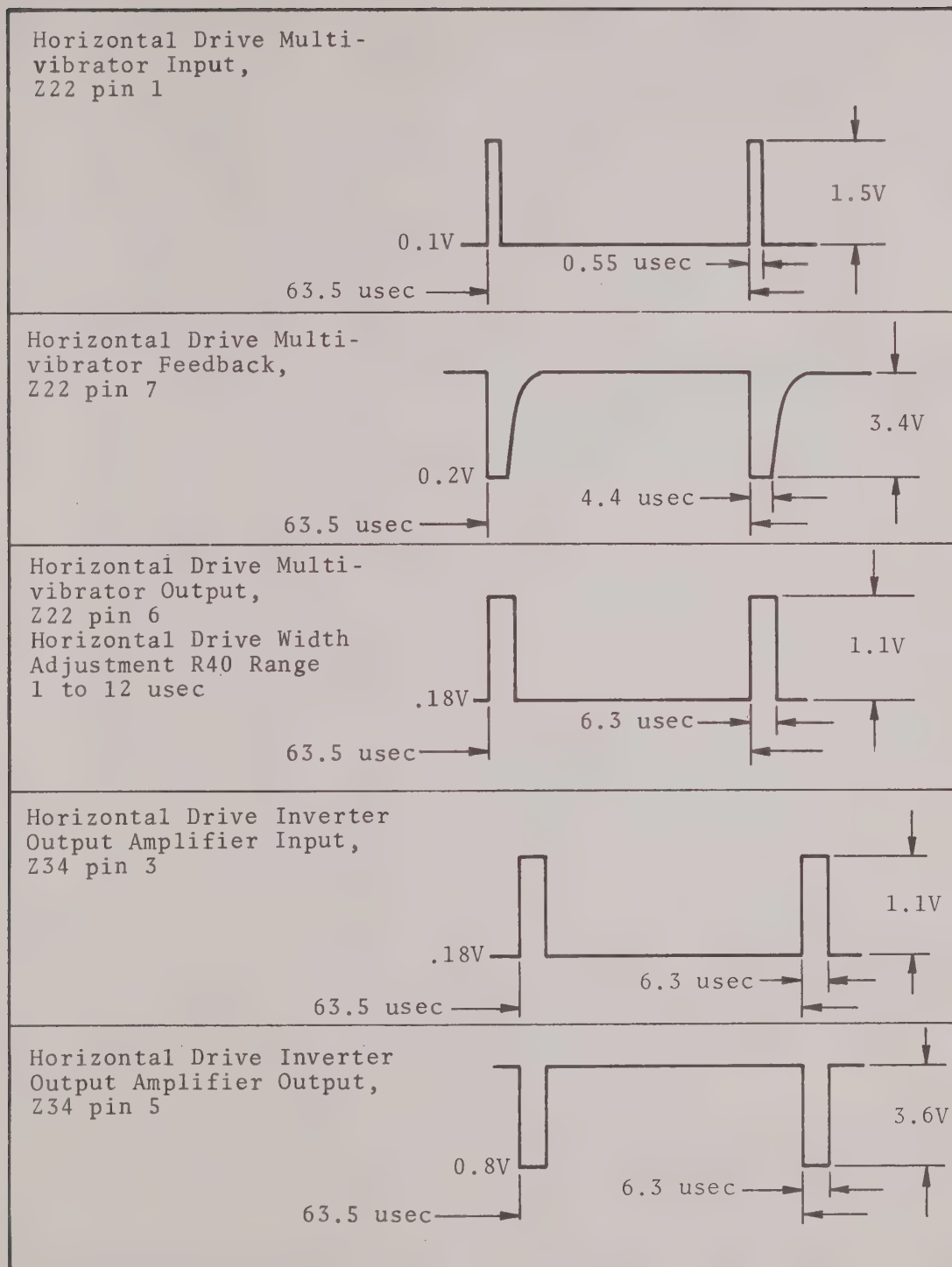


Figure 5-17. FR-10, FR-20 Horizontal Drive Circuit, Waveforms, 525 Line Rate.

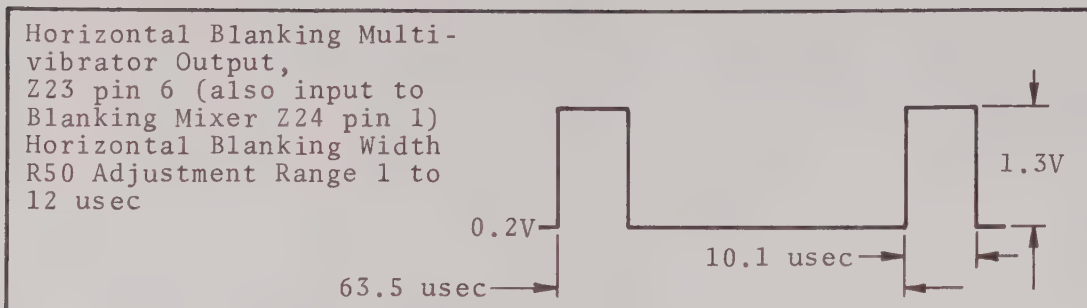


Figure 5-18. FR-10, FR-20 Horizontal Blanking Multivibrator Waveforms, 525 Line Rate.

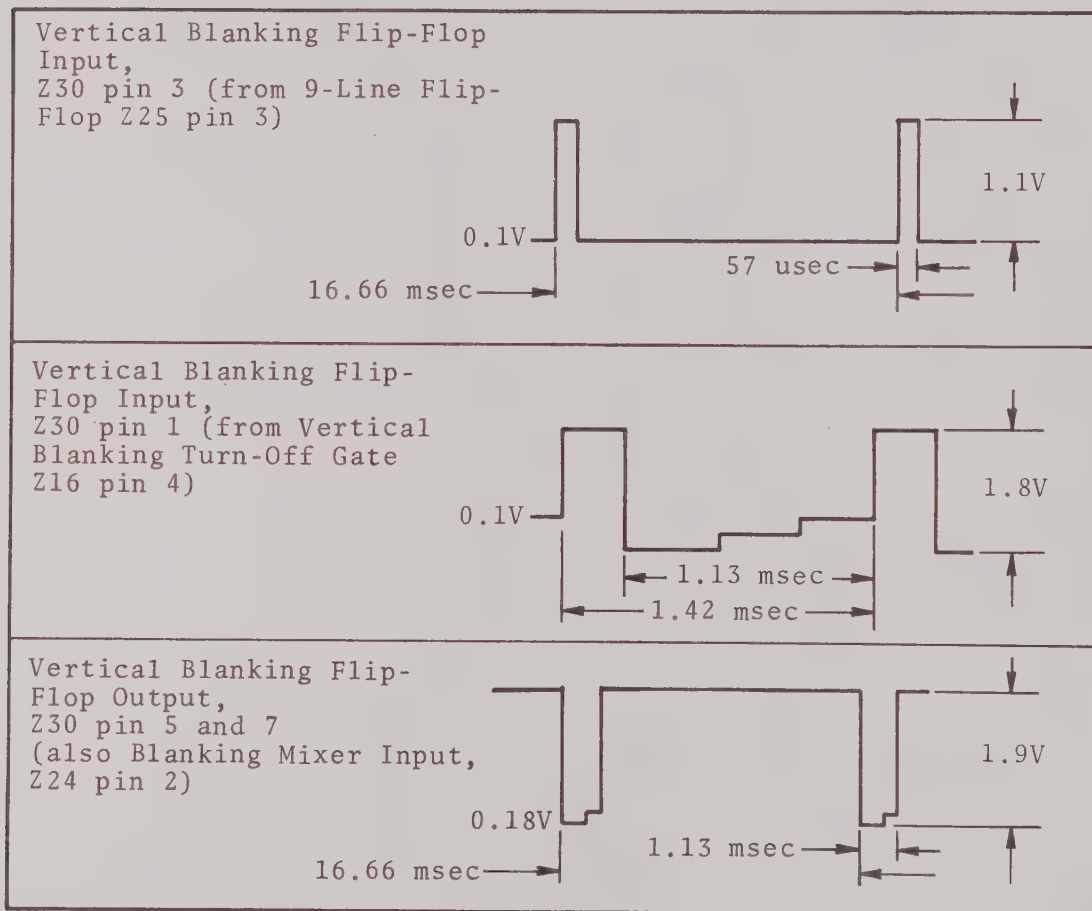


Figure 5-19. FR-10, FR-20 Vertical Blanking Flip-Flop Waveforms, 525 Line Rate.

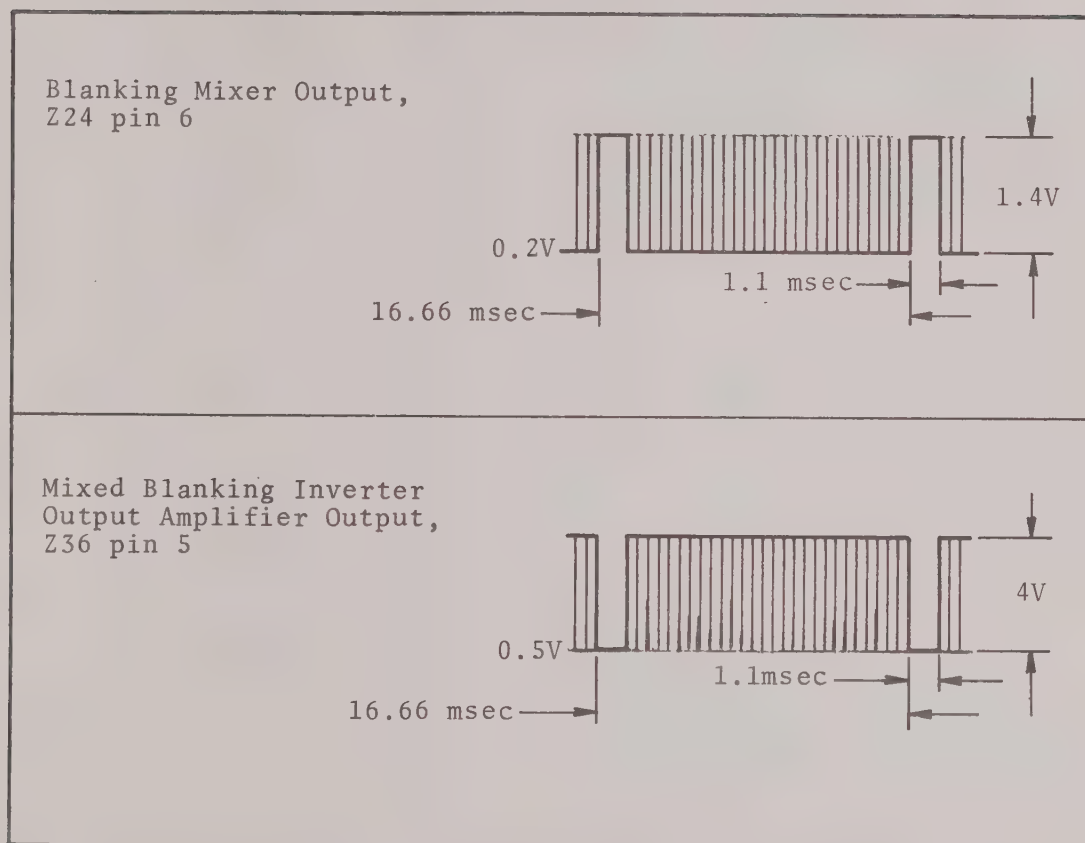


Figure 5-20. FR-10, FR-20 Blanking Mixer Output and Mixed Blanking Inverter Output Amplifier Waveforms, 525 Line Rate.

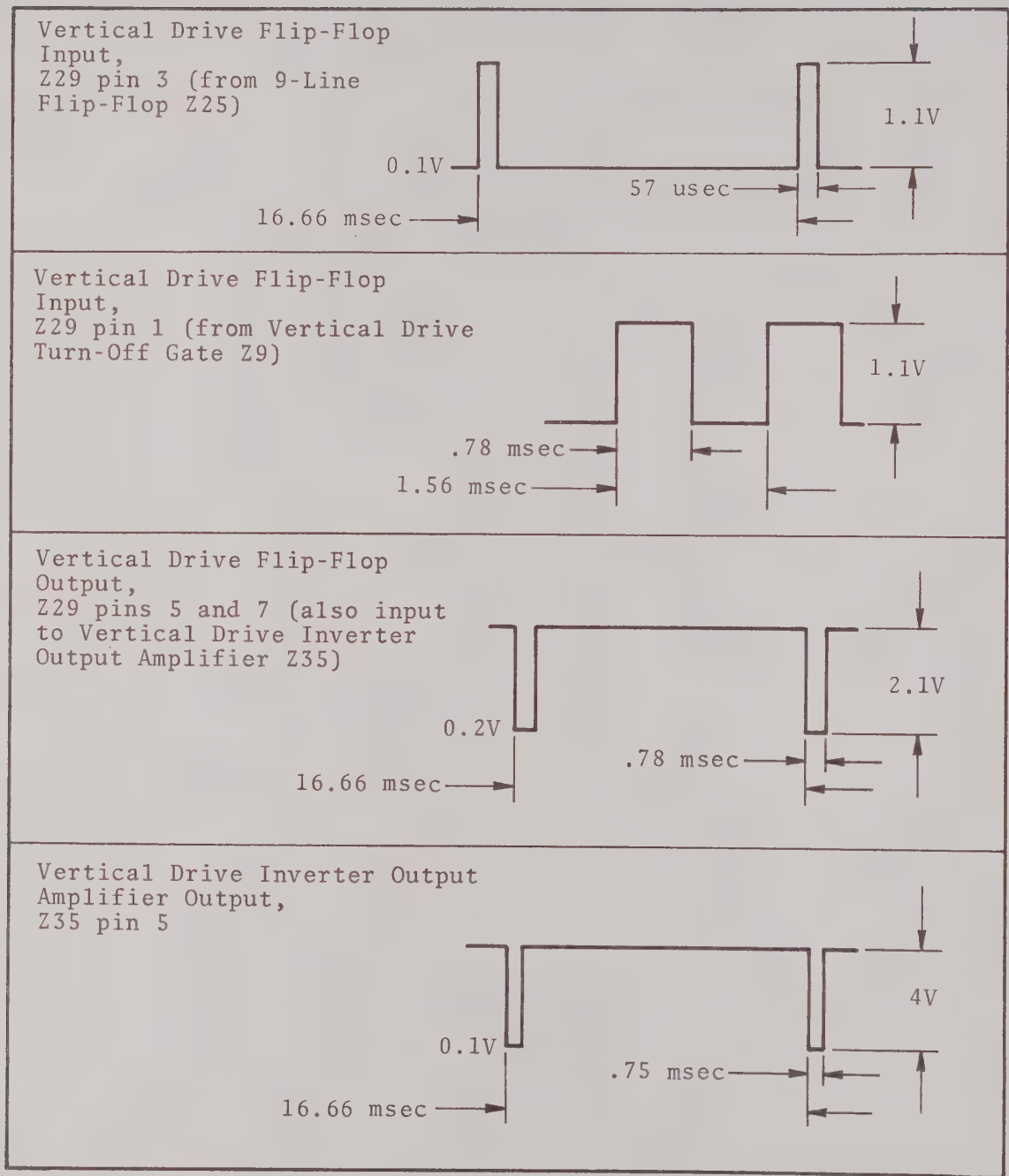
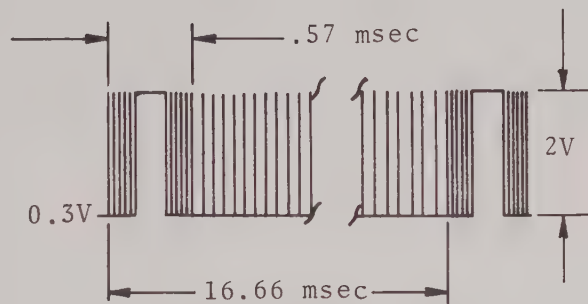


Figure 5-21. FR-10, FR-20 Vertical Drive Circuit Waveforms,
525 Line Rate.

Sync Inverter Output
Amplifier Input,
Z33 pin 3



Sync Inverter Output
Amplifier Output,
Z33 pin 5

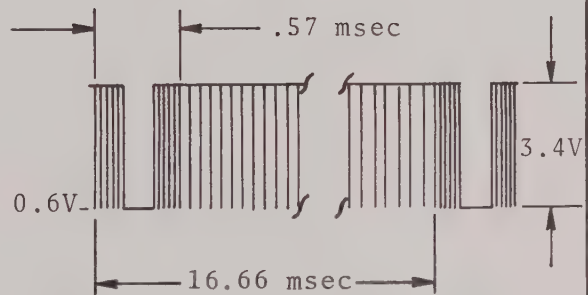


Figure 5-22. FR-10, FR-20 Sync Inverter Output Amplifier Waveforms, 525 Line Rate.

SECTION VI PARTS LIST

6-1. GENERAL

This section contains the maintenance parts list for the Fairchild Television Sync Signal Generator FR-20 and FR-20/C (P/N 9530 1561) and FR-10 and FR-10/C (P/N 8530 5331). In addition to the parts that are common to both the FR-10(C) and the FR-20(C), the list includes, for the FR-20, a power transformer, vertical phasing circuit, front panel test jacks, and rear panel coaxial connectors; these are identified by "(FR-20)" in the description column, and shown in the schematic diagram figure 6-2, sheet 2. All part numbers are Fairchild unless otherwise specified. Figure 6-1 shows parts location on the component board assembly (part number 8431 4391).

<u>REFERENCE DESIGNATION</u>	<u>PART NUMBER</u>	<u>DESCRIPTION</u>
----------------------------------	--------------------	--------------------

CAPACITORS

Note: All capacitors are fixed, mica, $\pm 5\%$, 500V, unless otherwise specified.

C1	0376 9320	Electrolytic, 200 uf, 10V
C2	0376 4210	3300 pf, 300V
C3	0376 4220	820 pf, 300V
C4	0327 6500	390 pf, 100V
C5	0376 4170	510 pf, 500V
C6 & C7	0376 4270	Ceramic, 0.01 uf, 50V
C8		Not used
C9	0376 4280	Ceramic, 0.02 uf, 50V
C10 thru C13	0376 4230	1500 pf, 300V
C14 thru C17	0376 4170	510 pf, 500V
C18 & C19	0376 4230	1500 pf, 300V
C20	0376 9320	Electrolytic, 200 uf, 10V
C21	0376 9310	Electrolytic, 1 uf, 40V
C22 & C23	0376 4290	Ceramic, 0.47 uf, 25V
C24 thru C26	0376 9310	Electrolytic, 1 uf, 40V
C27	0376 9300	Electrolytic, 10 uf, 25V
C28	0376 9390	Electrolytic, 640 uf, 25V
C29	0376 9320	Electrolytic, 200 uf, 10V
C30	0376 9390	Electrolytic, 640 uf, 25V
C31 & C32	0376 9320	Electrolytic, 200 uf, 10V
C33	0376 9330	Electrolytic, 20 uf, 16V
C34	0376 9340	Electrolytic, 640 uf, 6.4V
C35	0376 9390	Electrolytic, 640 uf, 25V
C36	0376 9290	Electrolytic, 1000 uf, 6.4V
C37	0377 1130	Film, 1.0 uf, 100V (FR-20)

DIODES

CR1 thru CR8	2600 9220	1N4384
CR9	2630 9250	Zener, 1N757A
CR10	2631 0750	Zener, 1N749A
CR11 thru CR16	2600 9220	1N4384

REFERENCE
DESIGNATION

PART NUMBER

DESCRIPTION

QUARTZ CRYSTAL UNIT

CR17**	2630 9180	Crystal, 31.5 Kc
	2631 1730	Crystal, 37.5 Kc
	2631 1740	Crystal, 52.5 Kc
	2631 1750	Crystal, 56.7 Kc
	2631 1760	Crystal, 61.74 Kc
	2631 1770	Crystal, 73.5 Kc

TERMINAL STUDS

E1 thru E23	5132 3370	Turret
-------------	-----------	--------

CONNECTORS

J1 thru J10	0936 3080	Jack, P.C., tp
J11	0936 2730	31 pin, female
P11*	0934 5541-1	525 lines/frame, male
	0934 5541-2	625 lines/frame, male
	0934 5541-3	875 lines/frame, male
	0934 5541-4	945 lines/frame, male
	0934 5541-5	1029 lines/frame, male
	0934 5541-6	1225 lines/frame, male
J12 thru J15	0936 3140	Connector, receptacle, coaxial (FR-20)
J16 thru J19	0935 9400	Jack, tp, teflon press fit, white (FR-20)
J20	0935 0410	Jack, tp, teflon press fit, black (FR-20)

MICROLOGIC INTEGRATED CIRCUITS

Z1	2630 9500	Type 914 (U5B991429X) (Metal Can)
Z2	2630 9360	Type 900 (U8B990028X)
Z3 thru Z8	2630 9650	Type 923 (U8A992328X)
Z9	2630 9550	Type 915 (U5F991529X)
Z10 thru Z15	2630 9650	Type 923 (U8A992328X)
Z16	2630 9550	Type 915 (U5F991529X)
Z17 thru Z26	2630 9510	Type 914 (U8A991428X)
Z27	2630 9550	Type 915 (U5F991529X)
Z28 thru Z30	2630 9510	Type 914 (U8A991428X)
Z31	2630 9360	Type 900 (U8B990028X)
Z32	2630 9510	Type 914 (U8A991428X)
Z33 thru Z36	2630 9360	Type 900 (U8B990028X)

* Only one supplied as required by lines/frame requirement.

** Optional. Paired with Resistor R24.

REFERENCE
DESIGNATION

PART NUMBER

DESCRIPTION

RESISTORS

Note: All resistors are fixed, composition, $\pm 5\%$, 1/4W unless otherwise specified. Resistances are in ohms; K = thousand, M = million.

R1	0235 4500	330
R2	0235 4730	3.3K
R3	0235 4780	5.1K
R4	0114 1190	Variable, wire wound, 10K, $\pm 10\%$, 2W
R5	0235 4460	220
R6	0235 4870	12K
R7	0114 0400	Variable, 10K, composition, 1/4W
R8	0235 4620	1K
R9 thru R11	0114 0400	Variable, 10K, composition, 1/4W
R12 thru R14	0235 4620	1K
R15 thru R18	0235 4710	2.7K
R19	0235 4810	6.8K
R20 thru R23	0235 4620	1K
R24**	0235 5060	75K (525 lines/frame)
	0235 5040	62K (625 lines/frame)
	0235 5000	43K (875 lines/frame)
	0235 4980	36K (945 lines/frame)
	0235 4970	33K (1029 lines/frame)
	0235 4950	27K (1225 lines/frame)
R25	0235 4810	6.8K
R26	0235 4540	470
R27	0235 4470	240
R28	0235 4570	620
R29 & R30	0235 4540	470
R31	0235 4400	120
R32	0235 4540	470
R33	0235 4400	120
R34	0235 4670	1.8K
R35	0235 4620	1K
R36	0235 5570	10M
R37	0235 5630	18M
R38	0235 5250	470K
R39	0235 4620	1K
R40	0114 0400	Variable, 10K, composition, 1/4W
R41	0235 4620	1K
R42	0235 4770	4.7K
R43	0235 4540	470
R44	0235 4870	12K
R45	0114 0400	Variable, 10K, composition, 1/4W
R46	0235 4770	4.7K
R47 thru R49	0235 4730	3.3K
R50	0114 0400	Variable, 10K, composition, 1/4W
R51 & R52	0235 4620	1K
R53	0114 1080	Variable, 25K, composition, 1/2W (FR-20)
R54	0203 0400	470, 1/2W

** Optional. Paired with Quartz Crystal Unit, CR17.

REFERENCE
DESIGNATION

PART NUMBER

DESCRIPTION

SWITCHES

S1	0533 5710	Rotary, 3P4P
S2 & S3	0533 5570	Toggle, DPDT (FR-20)

TRANSISTORS

Q1	2631 3510	2N3638A
Q10 thru Q14	2631 3540	2N3643
Q15	2631 3510	2N3638A
Q16 & Q17	2631 1480	Power, 40250V1
Q18	2631 3540	2N3643

MISCELLANEOUS (FR-20)

DS1	1231 8620	Indicator light, neon, red, built-in resistor
F1	1100 1070	Fuse, 1/4 amp
T1	2031 5341	Transformer, power, DE-23169
W1 & P1	5060 2540	Cable assembly, power, type STV-18/3
	0905 5140	Adapter, Power Connector 3 Prong

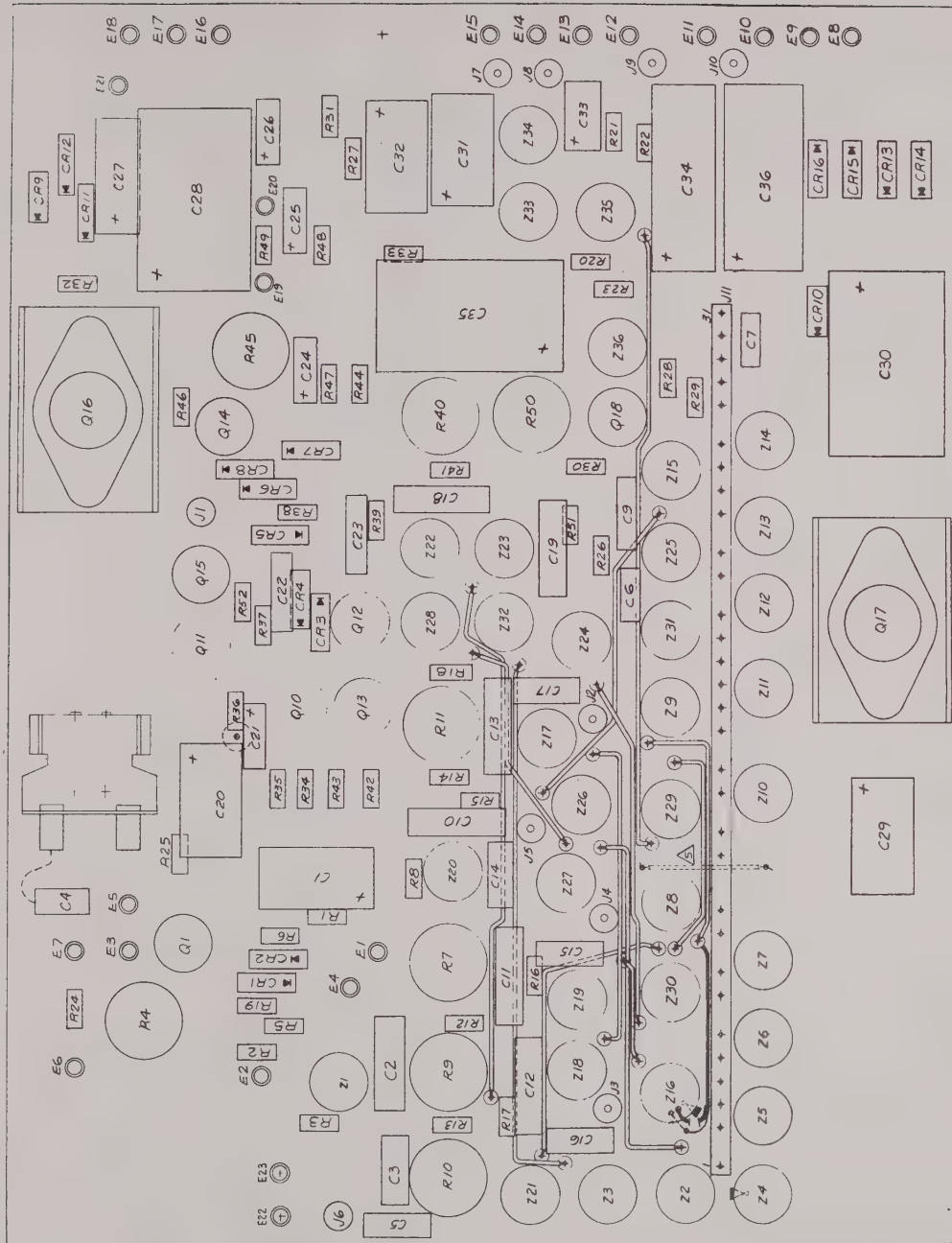


Figure 6-1. FR-10, FR-20 Component Board, Parts Location

NOTES:

- UNLESS OTHERWISE SPECIFIED:
RESISTANCE VALUES ARE IN OHMS $\pm 5\%$,
CAPACITANCE VALUES ARE IN MICROFARADS.

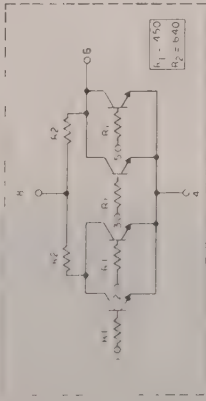
TABLE OF EIA PULSE WIDTHS IN MICRO SECONDS.

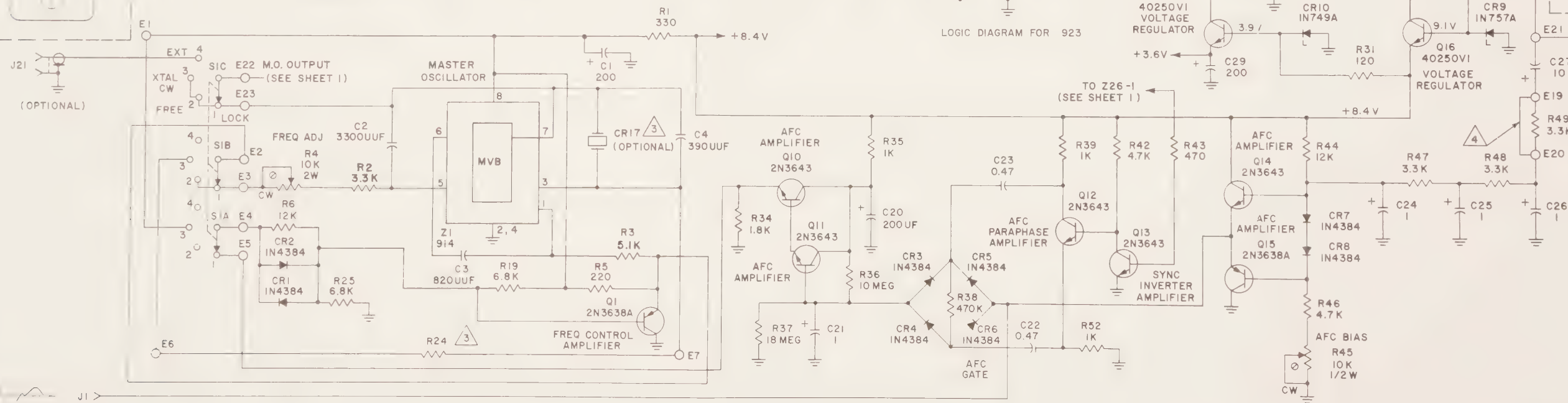
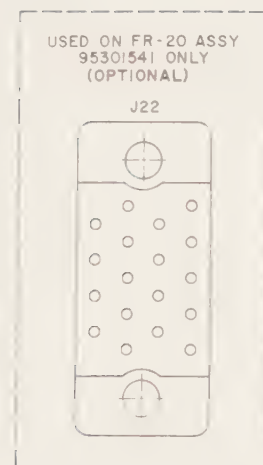
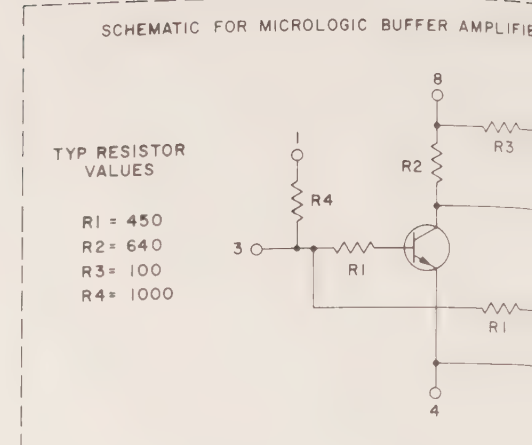
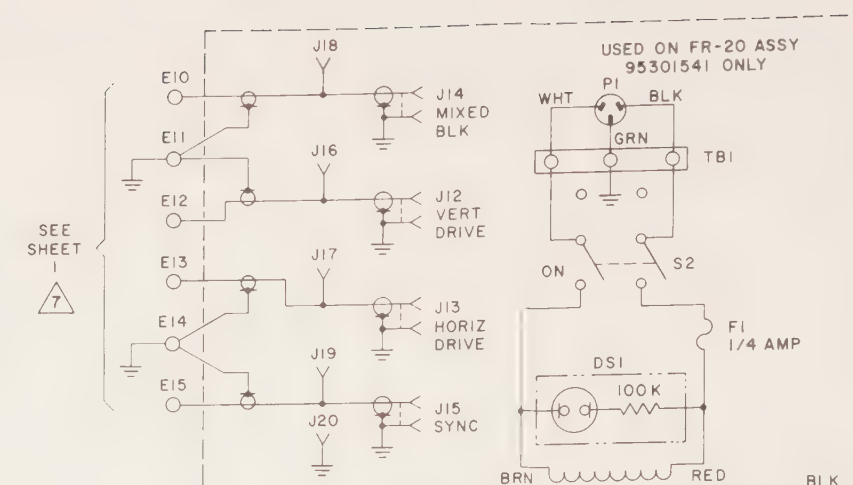
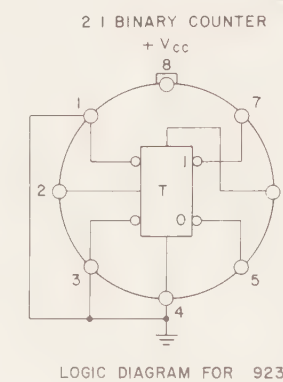
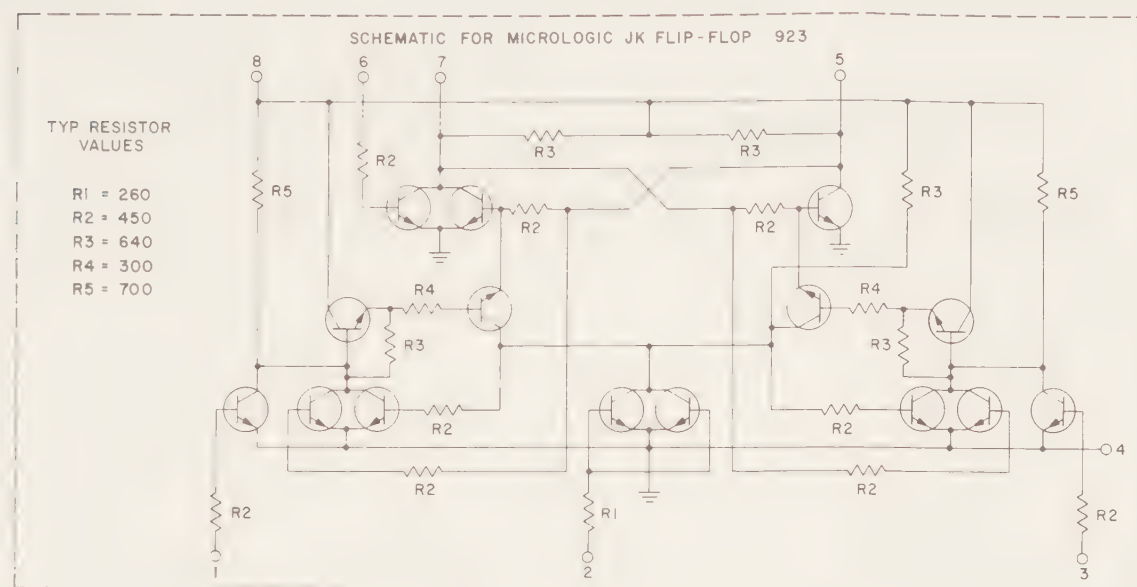
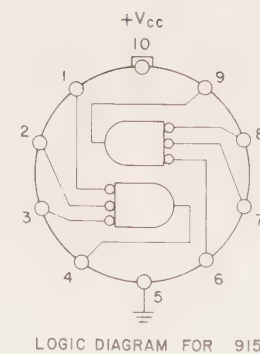
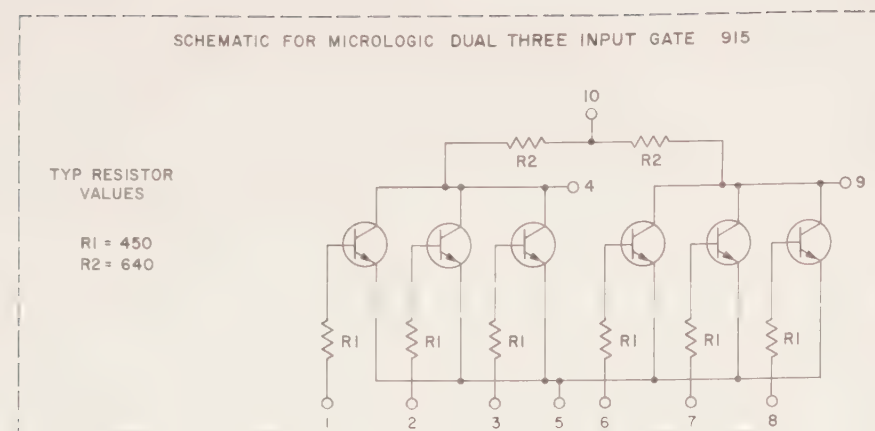
PUL PLUG NO.	LINE RATE	525	625	875	945	1029	1225
J6	MASTER OSC.	31.75	26.65	19.05	17.65	16.2	13.6
J9	VERTICAL DRIVE	762	641	686	635	585	653
J10	VERTICAL BLK	1143	1282	1370	1270	1170	1310
J8	HORIZ DRIVE	6.3	5.3	3.8	3.5	3.3	2.7
J10	HORIZ BLK	11	9	6.5	6	5.6	4
J2	HORIZ DRIVE	3	2.5	1.8	1.7	1.5	1.3
J3	HORIZ SYNC	4.4	3.7	2.6	2.4	2.2	1.9
J4	EQUALIZER STOP	6.7	5.6	4	3.7	3.4	2.9
J5	HORIZ SYNC STOP	9.1	7.6	5.5	5	4.6	3.9

3. SELECTED VALUE:

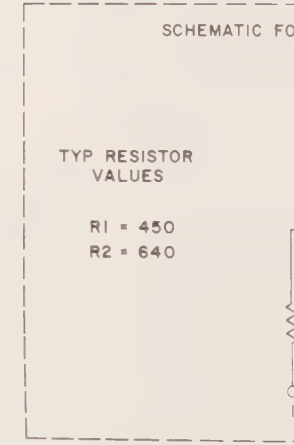
LINE RATE	CR17	R24
525	3.5 KC	75K
625	37.5 KC	65K
945	56.7 KC	45K
1029	61.74 KC	33K
1225	73.5 KC	27K

SCHEMATIC FOR MICROLOGIC 9.4





60 CPS RATE
3.5 VPP

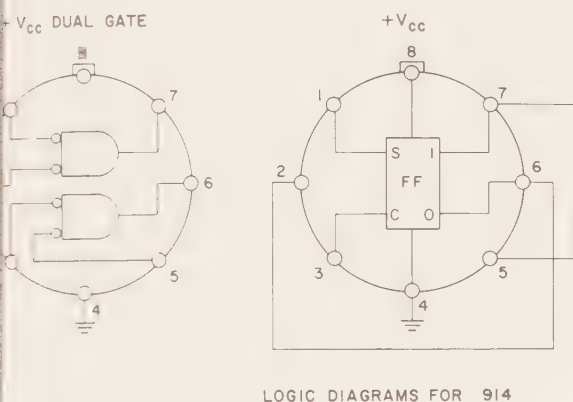
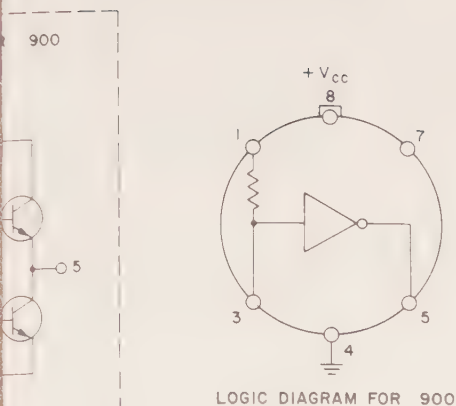


NOTES: (CONT.)

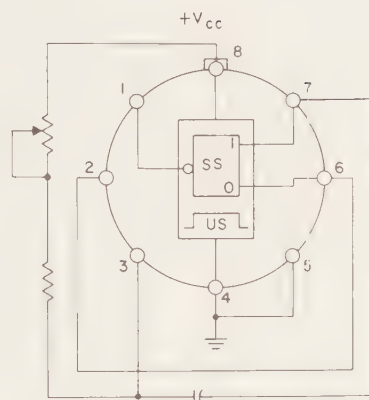
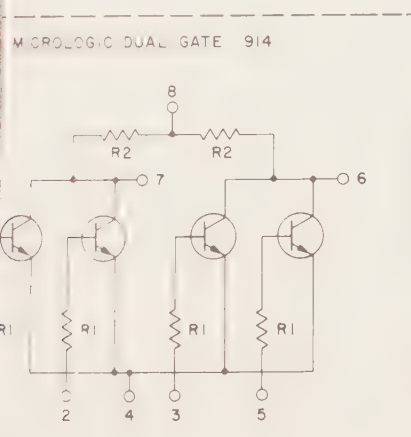


WHEN FR10 OR FR10/C IS USED IN TCS-950B
THE FOLLOWING CONNECTIONS ARE
MADE TO PRINTED CIRCUIT CONNECTOR P2:

E8 TO P2-9	E12 TO P2-5	E16 TO P2-13
E9 TO P2-10	E13 TO P2-7	E17 TO P2-11
E10 TO P2-1	E14 TO P2-4	E18 TO P2-12
E11 TO P2-2	E15 TO P2-3	

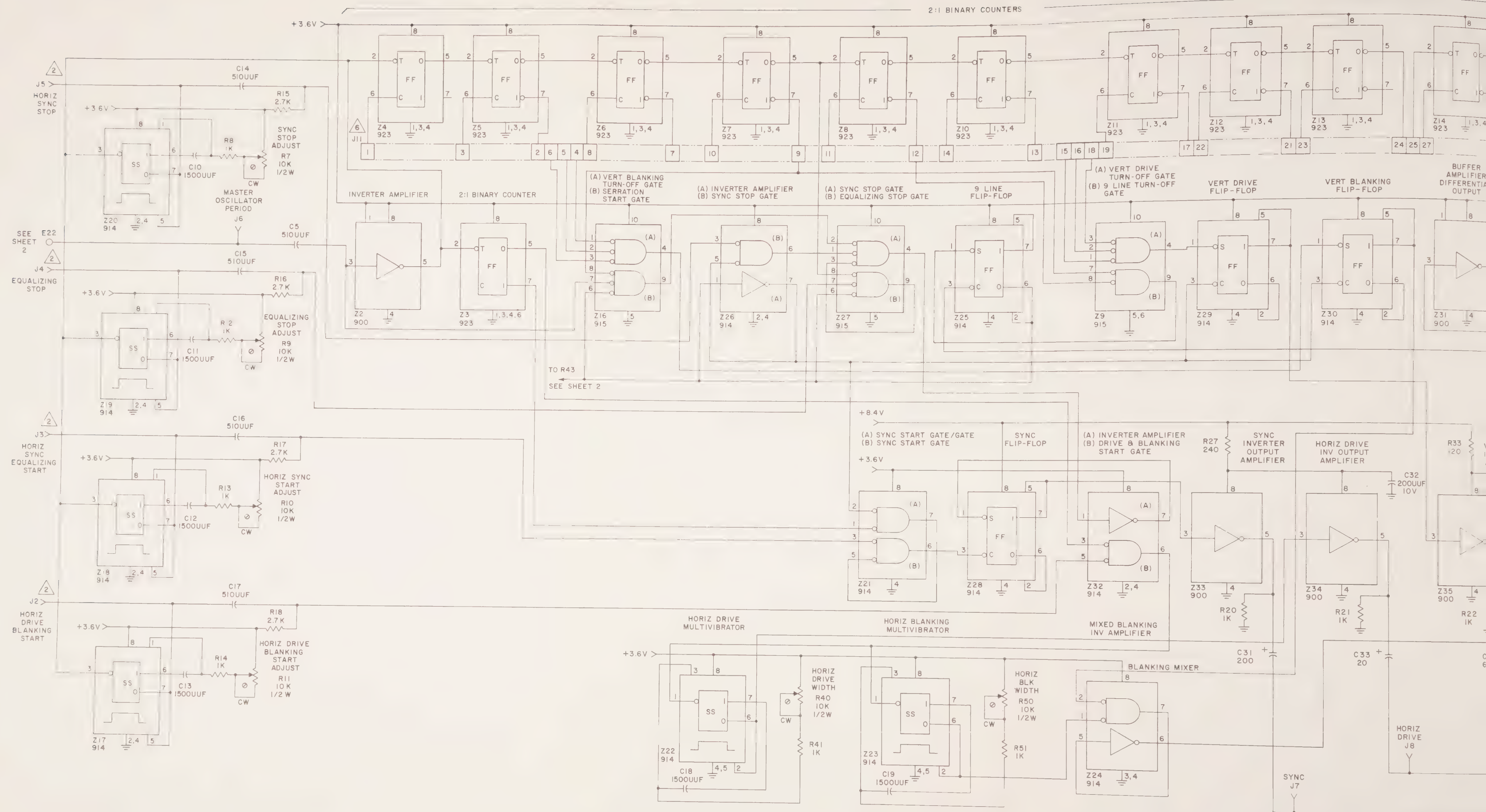


MICROLOGIC 914 MAY BE CONFIGURED FOR USE AS A
MULTI-VIBRATOR (MVB), SINGLE SHOT MULTI-VIBRATOR (SS),
FLIP-FLOP (FF), AND INVERTER AMPLIFIER.



DWG 66325411 REV D

Figure 6-2 FR-10, FR-20 Television Sync Signal Generator
Schematic Diagram (Sheet 2 of 2)



NOTES:

1. UNLESS OTHERWISE SPECIFIED:
RESISTANCE VALUES ARE IN OHMS, $\pm 5\%$.
RESISTORS ARE 1/4 WATT.
CAPACITANCE VALUES ARE IN MICROFARADS.

2. TABLE OF EIA PULSE WIDTHS IN MICROSECONDS.

P11 PLUG NO.			09345541-1	09345541-2	09345541-3	09345541-4	09345541-5	09345541-6	09345541-7
LINE RATE			525	625	875	945	1029	1225	521
J NO	FUNCTION	R NO							
J6	MASTER OSCILLATOR PERIOD	R4	31.75	26.65	19.05	17.65	16.2	13.6	33.26
J9	VERTICAL DRIVE WIDTH	FIXED	762	641	686	635	583	653	SEE 525 COLUMN FOR PULSE WIDTHS
J10	VERTICAL BLANKING WIDTH	FIXED	1143	1282	1370	1270	1170	1310	
J8	HORIZONTAL DRIVE WIDTH	R40	6.3	5.3	3.8	3.5	3.3	2.7	
J10	HORIZONTAL BLANKING WIDTH	R50	11	9	6.5	6	5.6	4	
J2	HORIZONTAL DRIVE & BLANKING START	R11	3	2.5	1.8	1.7	1.5	1.3	
J3	HORIZONTAL SYNC & EQUALIZING START	R10	4.4	3.7	2.6	2.4	2.2	1.9	
J4	EQUALIZING STOP	R9	6.7	5.6	4	3.7	3.4	2.9	
J5	HORIZONTAL SYNC STOP	R7	9.1	7.6	5.5	5	4.6	3.9	

3. SELECTED VALUE:

LINE RATE	CR17	R24
525	31.5 KC	75K
625	37.5 KC	62K
875	52.5 KC	43K
945	56.7 KC	36K
1029	61.74 KC	33K
1225	73.5 KC	27K
521	31.25 KC	75K

4. CUT OUT JUMPER WHEN FR-10 OR FR-10/C IS USED IN TCS-950B

5. REMOVE JUMPER WIRE WHEN USED ON FR-20

6. CONNECTIONS TO J11 ARE JUMPED IN ATTACHED P11, AS SHOWN BELOW:

525 LINES / FRAME	625 LINES / FRAME	875 LINES / FRAME	945 LINES / FRAME	1029 LINES / FRAME	1225 LINES / FRAME
1-30	1-30	1-11-14-19-20-23-27	1-30	1-30	1-30
2-29	2-29	2-NC	2-29	2-29	2-29
3-6-10-11-14-15-18-22-27-31	3-8-10-11-14-20-22	3-30	3-6-10-14-18-19-22-31	3-6-10-11-18-19-23-31	3-8-10-11-20-22-23
4-12	4-6-15-18-19-23-27-31	4-13-16	4-13-16	4-13-16	4-6-14-15-18-19-27-31
5-13-16	5-17	5-17	5-17	5-17	5-21
7-NC	7-NC	6-8-10-18-22-31	7-NC	7-NC	7-NC
8-19-20-23	9-NC	7-29	8-11-20-23-27	8-14-20-22-27	9-NC
9-NC	12-NC	9-NC	9-NC	9-NC	12-NC
17-NC	13-16	12-15	12-15	12-15	13-NC
21-NC	21-NC	21-NC	21-NC	21-NC	16-17
24-26	24-26	24-25	24-25	24-25	24-25
25-NC	25-NC	26-28	26-28	26-28	26-28
28-NC	28-NC				

NOTES CONTINUED ON SHEET 2

SEE SHEET 2

7

DWG 66325411 REV H

Figure 6-2 FR-10, FR-20 Television Sync Signal Generator Schematic Diagram (Sheet 1 of 2)

APPENDIX A

LOGIC AND LOGIC CIRCUITS

1. GENERAL

Logic refers to that type of digital circuitry which uses only two signal levels in its operation. The two signal levels are called "high" and "low" when referring to relative voltages, "on" and "off" in switching actions, "one" and "zero" in binary form, and "X" and " $\bar{X}$ " (not X) in Boolean form.

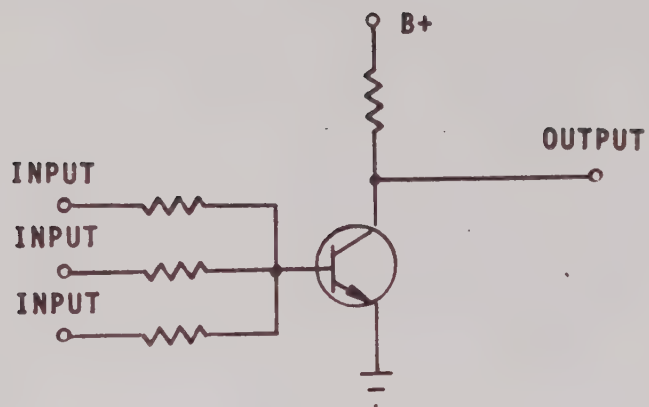
2. GATES

A basic logic gate is shown in figure A-1. The circuit consists of a transistor, three base resistors, and a collector load resistor. In operation, if any one input is high, the transistor will saturate, causing the output to be low (near ground). Conversely, all inputs must be low for the output to be high. This circuit may be considered either a NAND or NOR gate depending on the function (the logic symbols shown are based on MIL-STD-806B). The circle at the output of the NOR gate indicates that the activated state is low. The circles at the inputs of the NAND gate indicate that the inputs must be low to activate the gate.

3. MULTIVIBRATORS

Two gates can be connected to form a bi-stable multivibrator (flip-flop) as shown in figure A-2. A flip-flop is also shown in logic diagrams as the rectangular symbol shown next to the gates.

Gates can be connected to form monostable and astable multivibrators as shown in figure A-3. The base diagram and elements of a Fairchild UL914 is shown in this example.



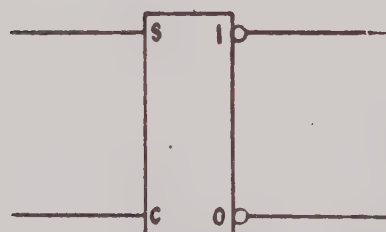
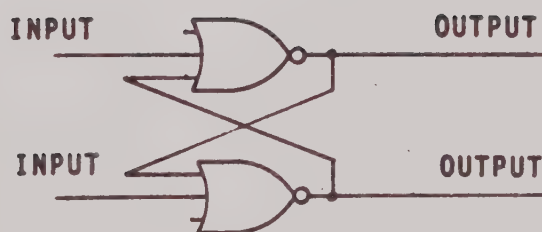
NAND GATE SYMBOL



NOR GATE SYMBOL

0000-1

Figure A-1. Basic Logic Gate



FLIP-FLOP SYMBOL

0000-2

Figure A-2. Bi-stable Multivibrator

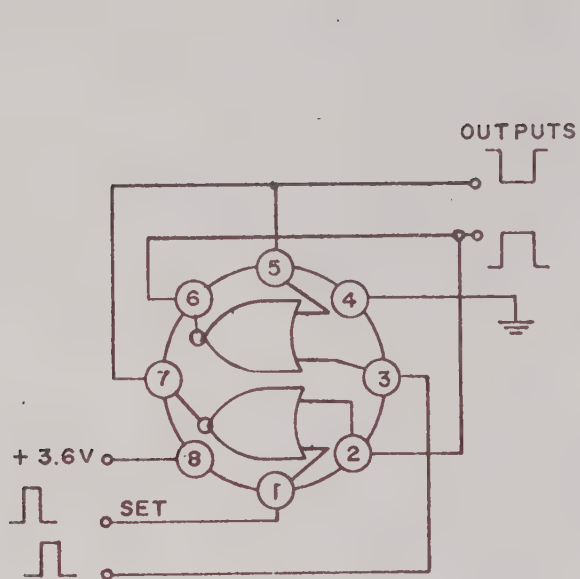
4. COUNTERS

Flip-flops are also available with a trigger input. A signal applied to the trigger input will change the flip-flop to its alternate state. This feature permits flip-flops to be used as a binary counter as shown in figure A-4. The base diagram and elements of a Fairchild UL923 is shown in this example.

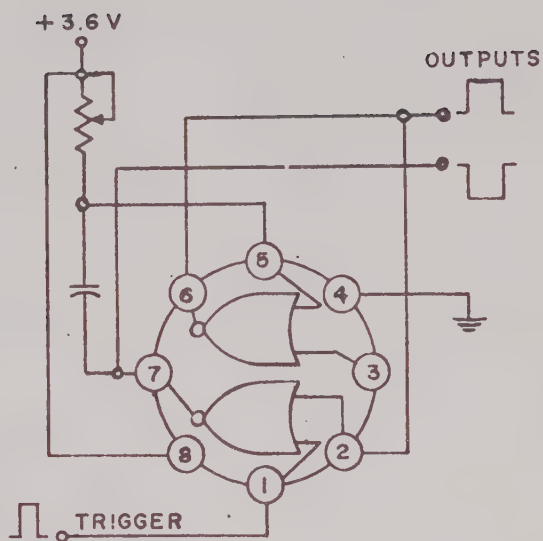
5. FAIRCHILD MICROLOGIC[®]

Control and counter circuits in the Models FR-10 and FR-20 use the following type integrated circuits (Micrologic) manufactured by Fairchild Semiconductor.

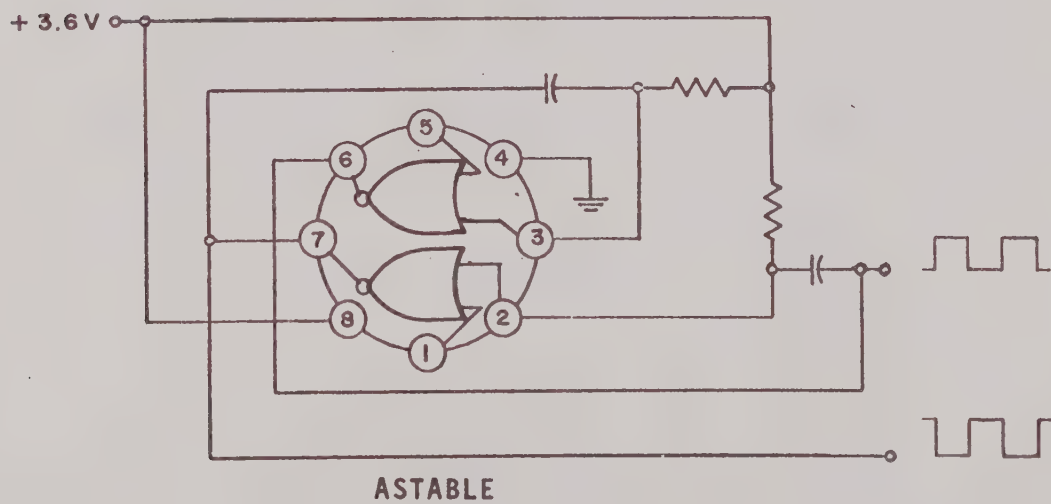
- a. UL900. This element contains a single medium power buffer inverter (figure A-5).
- b. UL914 is a dual 2-input gate (figure A-6).
- c. UL915 is a dual 3-input gate (figure A-7).
- d. UL923 is a JK flip-flop (figure A-8). This flip-flop differs from the RS flip-flop in that no ambiguous output state will result from simultaneous "one" inputs. The output state will reverse regardless.



BISTABLE



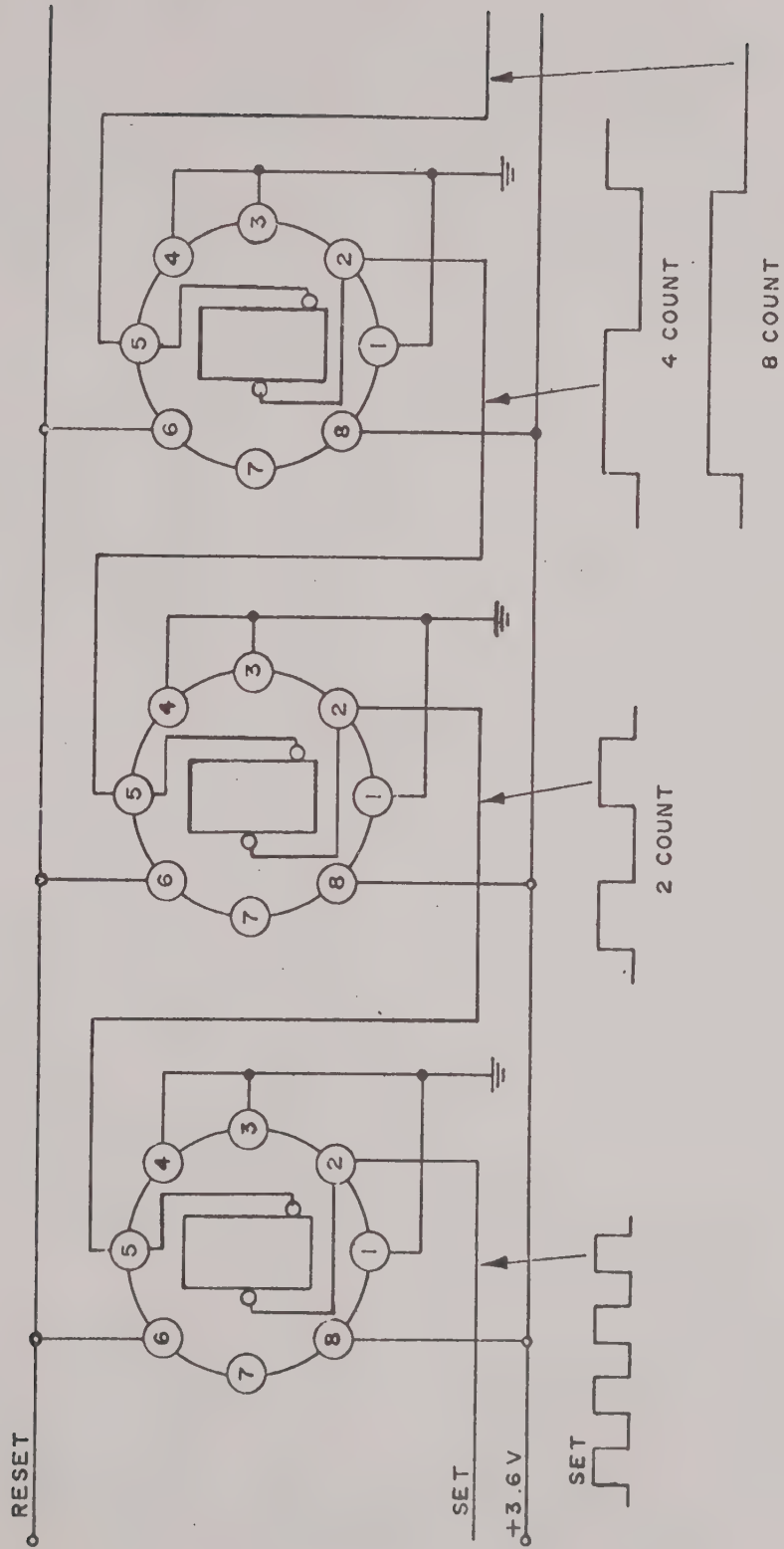
MONOSTABLE



ASTABLE

0000-3

Figure A-3. UL914 Multivibrators



0000-4

Figure A-4. Binary Counter

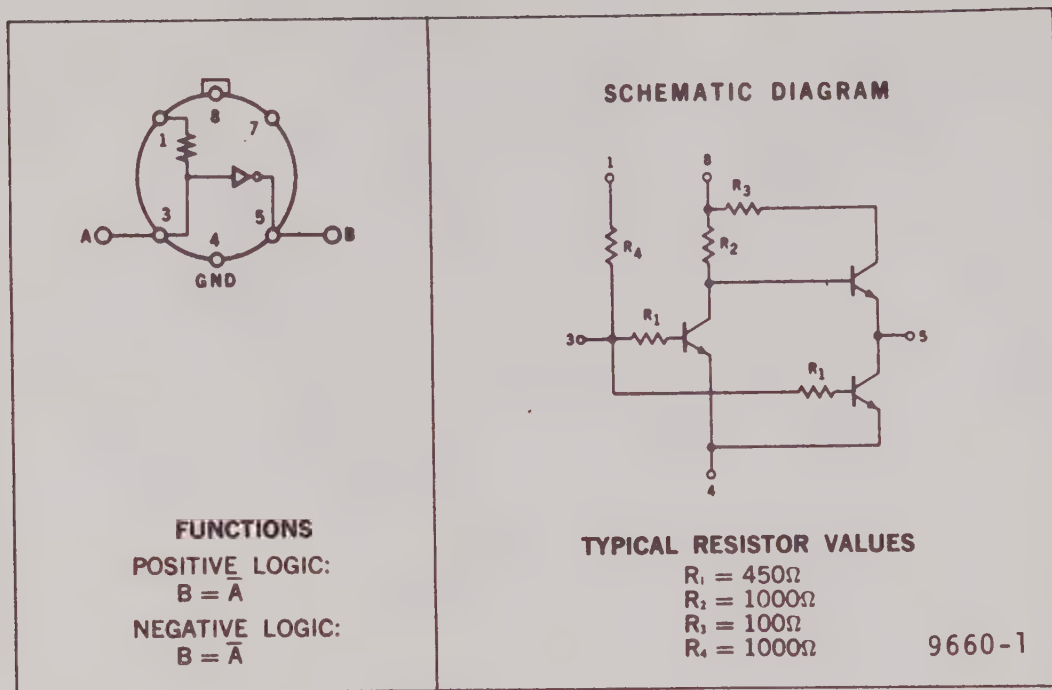


Figure A-5. Fairchild UL900 Buffer Inverter

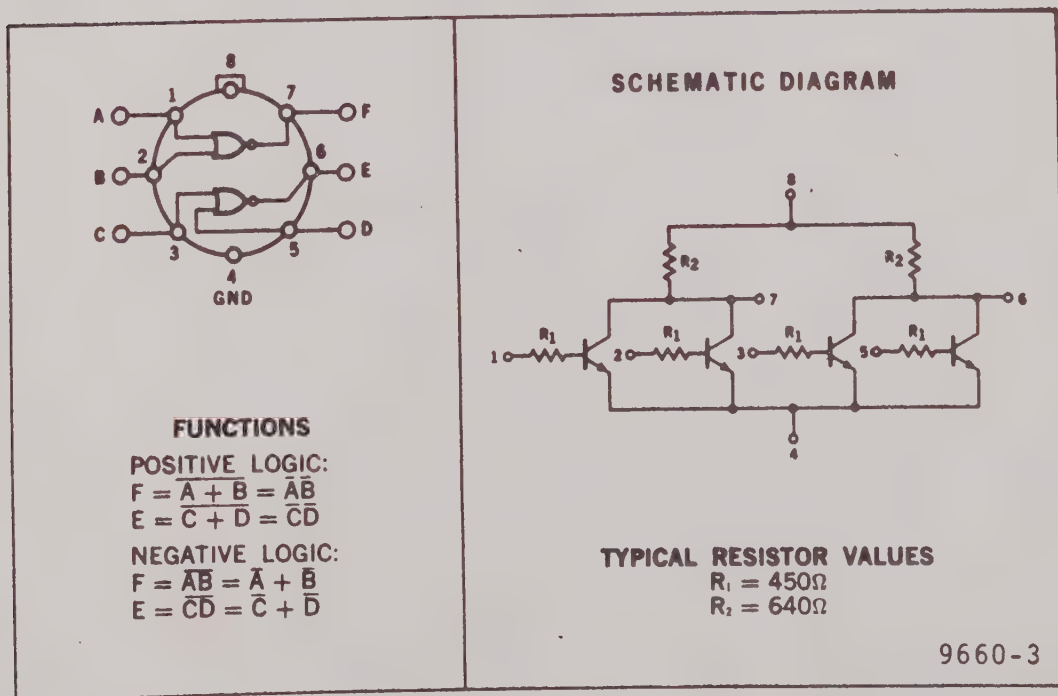


Figure A-8. Fairchild UL914 Dual 2-Input Gate

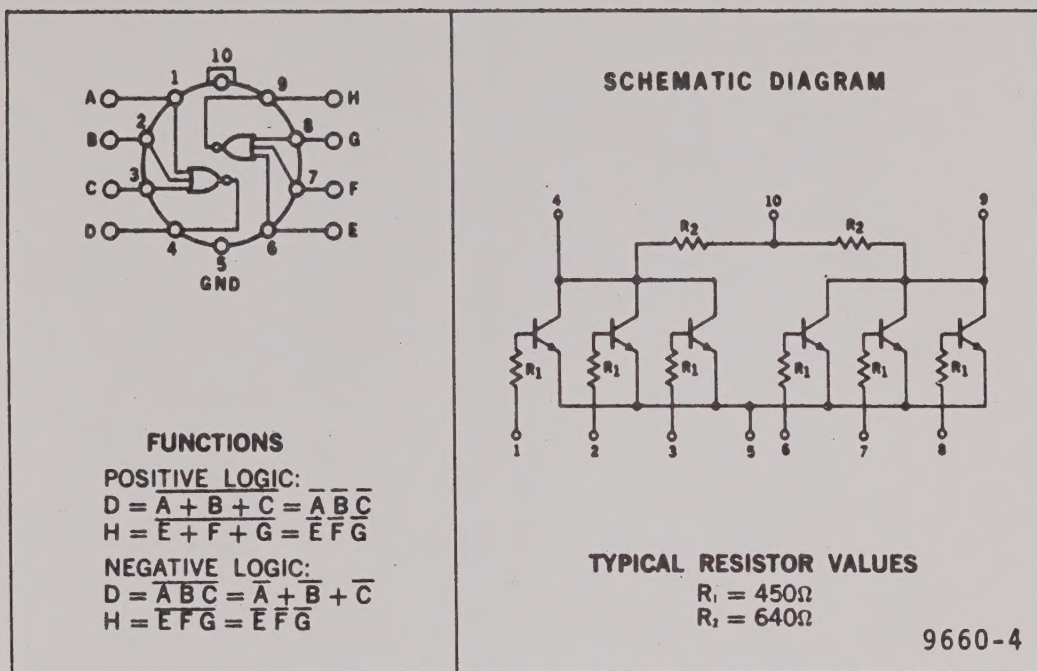


Figure A-7. Fairchild UL915 Dual 3-Input Gate

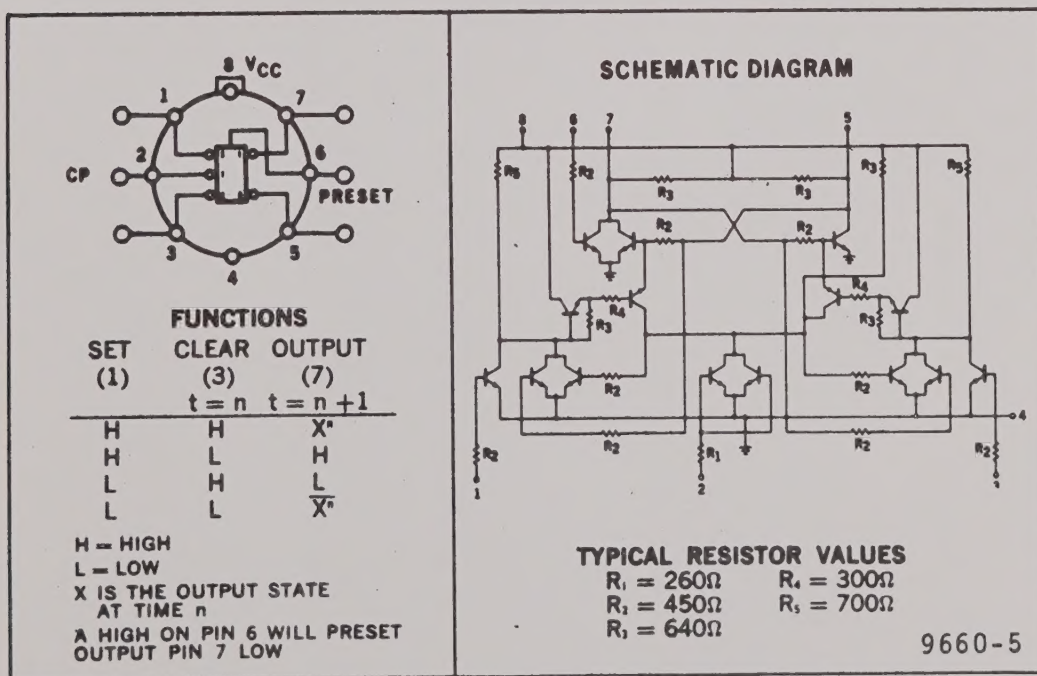


Figure A-8, Fairchild UL923 JK Flip-Flop

MP MASTER



MA30017